2005 Future Energy Challenge Competition

Topic B: Utility Interactive Inverter System for Small Distributed Generation

FINAL REPORT
On
1kW Interactive Inverter System for Unity PF Load

Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology
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1 ABSTRACT

Renewable energy sources are becoming very popular all over the world as an alternate to the conventional one, made from natural resources (fossil fuels, etc.). So there is huge extent of works to be done in converting the variable DC voltage generated by sources like solar cells, etc. to a fixed DC and/or AC voltage. Our proposal of a utility interactive inverter system will prop up such works immensely. Here we have proposed a scheme, based on the use of conventional DC-DC converter, followed by a PWM inverter, for generating an output waveform having low Distortion Factor (DF). A constant output voltage is assured by varying the modulation index of the PWM pattern, which is fed to the gate of the inverter. The output voltage is synchronized with the grid voltage by using Phase-Locked Loop (PLL). Standalone operation is performed by detecting the abnormal grid condition. The scheme is tested both for 110V (50Hz) and 240V (60Hz) output. The efficiency is around 85% and hopefully it can be improved by identifying the components, where the loss is incurring.

2 TEAM INFORMATION

At the beginning of this project we formed two teams to work in two schemes. When we selected the final scheme, two teams were merged to work in that scheme. Each student was assigned to his specific part in the project. All the students performed in this project are in undergraduate level and they have excellent result and reputation. Our team has two advisors who helped us in all matters. They are **Prof. Enamul Basher** (Dept. of EEE, BUET) and **Prof. Md. Rezwan Khan** (Dept. of ECE, UIU, Bangladesh). Besides these, **Ahmad Ehteshamul Islam**, ex-lecturer of Department of EEE, BUET helped the team in their work and coordinated their works. Team information is given below:

Name	Part of the Project Handled
K. M. Masum Habib	DC-DC Converter, PWM Inverter & Control System
(Student Team Leader)	
Rajib Mikail	DC-DC Converter, PWM Inverter & Control System
Md. Itrat Bin Shams	Sensors, Interfacing
M. S. Hossain	DC-DC Converter
Md. Ariful Haque	Interfacing
Toufiqul Islam	PWM Inverter, Sensors & Interfacing

The student team has been provided with an appropriate level of lab technicians to assist them in instrument handling. They have been working in an electronics lab of the department, which are well equipped with DC Power Supplies, Digital Oscilloscope, Circuit Simulators, etc.

3 TIMELINE

At the beginning of this project we demonstrated a time line for our work over the specified course of time. And throughout the project, we tried to follow the time line so far as possible. Adjustments in the scheduled plan were also made as necessary.

After our project was approved by the FEC authority back in May 2004, we started collecting our fund from our university and other sources. In this respect, we concentrated on gathering the parts from the companies, rather than collecting money. The backbone of our schemes was designed within May 2004 to June 2004. During the designing period, we also simulated our schemes for obtaining the theoretical modifications necessary.

We started to build our prototype from August 2004 and the work under one scheme was almost accomplished. The specifications that had been fulfilled were tested and reported here. After submitting the second progress report we performed some necessary testing. Then we prepared the final progress report and submitted it. As our team was busy with semester final exam, we started to work again from the 2nd week of May 2005. By this time we designed PCB, made some adjustments to our project and prepared the final report. Now we have finished our work and happy to submit the report and results related to this project.

4 INTRODUCTION

In recent years, the distributed generation system using new energy sources has attracted much attention [1]. Adverse impact of conventional energy resources on the environment has prompted the scientists and technologists to think of wider application of renewable energy sources like solar cell, fuel cell, etc. Since this distributed generation system links to a commercial source, a utility interactive inverter is required. In this case, some different levels of DC voltage are applied

as the input for the inverter because there are new energy sources such as solar batteries and fuel cells, and they provide different DC voltage levels. Such voltage is also power constrained and often limited by other environmental factors leading to instantaneous limitations in maximum voltage and/or current. This initiates the need of the development of a utility interactive inverter system, which will have low harmonics in the output voltage. Such a low harmonic in the output voltage, along with less weight for the inverter, will enable them to be used in advanced applications e.g. in satellites.

In general, the function of an Interactive Inverter system is to convert the DC output power from a renewable energy system, generating DC voltage within a certain range, to regulated AC power. There may be two stages of power converters. A DC-DC converter converts the low voltage DC output to a level at which an inverter can safely operate. Then inverter is used to invert the DC output from the DC-DC converter to a suitable AC voltage. The control unit of such an interactive system is required to ensure the following characteristics:

- Ability to produce constant output with an allowable variation for input DC voltage.
- Controllability of output voltage
- Availability of isolated operation and line parallel operation
- Low output harmonics
- High efficiency

The objective of the Utility Interactive Inverter Challenge is to develop a 1kW low-cost, low-weight inverter system that can synchronize itself with a unity power factor grid. It is required also to sense any abnormal operations like, blackouts and the system is required to disconnect form grid and supply a standalone load. The target cost of the stand-alone unit is less than $200 in high volume. Further, emphasis is also placed on high efficiency and controllability of the system.

For meeting the requirements of 2005 IFEC's quest, team from BUET started working with two schemes. One was based on the use of DC to high-frequency AC converter, a transformer for stepping up that high frequency AC, an ABS (absolute) circuit, along with a PWM inverter, for generating an output waveform having low Distortion Factor (DF). Another scheme involved an inverter system, in current controlled mode, for generating a very high resolution stepped sinusoidal current through the primary coil of a transformer. When the secondary coil will be

connected across a resistive load, the output voltage will also be stepped sinusoid; with of course some ripples. Both of the schemes seemed to be promising during the design and simulation stages. But after implementation of those designs we have finally come up with a scheme, giving comparably better performance. The output of first scheme, which is providing better performance, is found to comply with most of the IFEC requirements.

The organization of this final report is as follows. First, we will describe our schemes, using appropriate block diagrams. Along with that, reasons will be mentioned for dropping one of the schemes. For the chosen scheme between the two, the design and simulation results will be provided later. Next photographs of experimental setups will be provided, along with different experimental readings. Later on, the performance of the finally prepared prototype will be evaluated.

5 SCHEME EVALUATION

As mentioned earlier, BUET team started to work with two schemes. In this chapter, an overview of scheme that is not selected and reasons of its failure will be provided and the finally selected scheme will be covered in depth with necessary block diagrams and appropriate analysis.

5.1 DESCRIPTION OF SCHEME 2 AND REASONS FOR ITS FAILURE

The scheme is shown in Fig. 5.1.1. The input DC voltage, having value in the range of 30~60V is directly used for driving an H bridge inverter. As the current flowing through this primary winding, hence through the unity pf load, is a stepped sinusoid, so the voltage across the load will also be a stepped sinusoid.

A square wave (normal and inverted form) having of frequency 50~60 Hz (equal to the frequency of the grid) is used as one input to the AND gates shown. The other input to each of the AND gates comes from a comparator, which compares the output of a non-linear DAC (which controls

the current level) with the voltage across a sense resistor, used for sensing the load current. The output of the AND gate is then be fed to control the upper switches of the bridge. And the lower switches of the bridge are directly controlled by the original square wave. The input to the DAC comes from an Up/Down Counter.

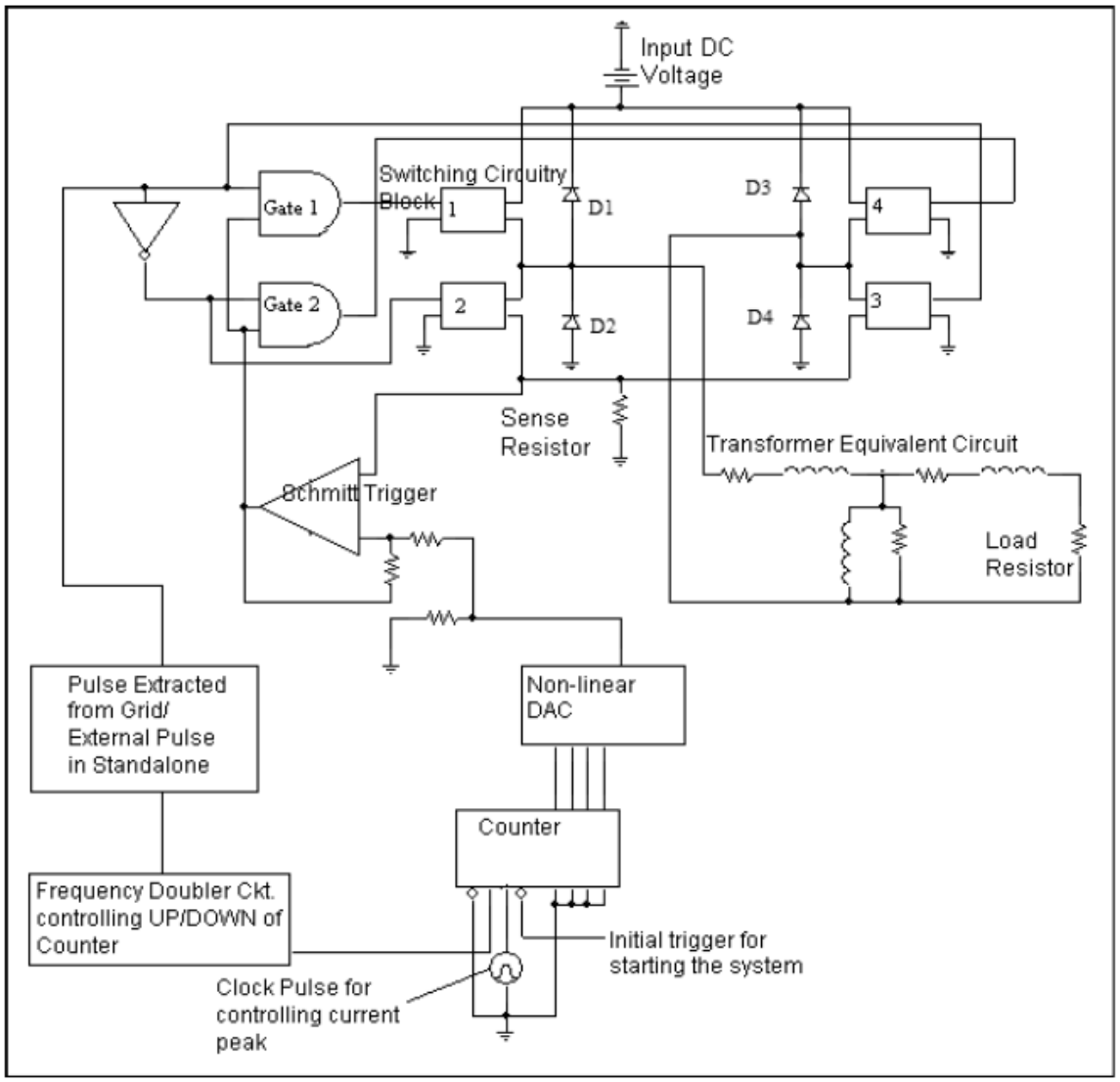


Fig. 5.1.1: Block Diagram of Scheme 2.

The counter's Up/Down pin is controlled by a square wave (synchronized with the previously used square wave), whose frequency is twice the frequency of the grid. And the clock frequency of the counter will depend on the desired resolution (the resolution is currently set to 16 steps in one half-cycle of the Current waveform). Now during the positive cycle of current through the inductor, AND gate 2 is always OFF and Transistor (Q3) is ON. So when the counter counts up

from zero, both inputs of AND gate 1 are HIGH. This turns ON Q1, thus passing current through load in positive direction. As a result, voltage across the sense resistor increases, and when it reaches the value set by DAC, the AND gate 1's output becomes LOW. Then load current free-wheels through D2 and Q3. Thus as the Counter counts UP, the output of DAC will increase non-linearly, and consequently increases the current through the load in a controlled manner. When the counter counts a maximum, such that current reaches its maximum, it will start to count DOWN. Hence the load current will start to decrease. When Counter counts zero, it will start to count UP again. This time AND gate 2 and transistors Q2 and Q4 will be in operation and the considered current will be negative.

As the inverter is operated in current controlled mode, so the maximum voltage across the sense resistor will change with change in load. Hence the maximum COUNT value of the Counter will be required to be adjusted with change in load, which can be easily done by changing the clock frequency of the Counter. As for example, the current through the sense resistor, hence through the load, can be decreased by decreasing the clock frequency.

The reasons for not finally selecting this circuit are:

- It became difficult for us to synchronize between different pulses used, which is essential for proper operation.
- The loss inside the sheet-silicon steel transformer was found to be excessive and was difficult to minimize.
- The weight of the transformer makes the overall weight of the system exceeding the competition limit.

5.2 FINAL SCHEME

In this section, an overview of the final scheme will be provided with necessary block diagrams and appropriate analysis. And then detailed analysis of each block will be given.

5.2.1 BLOCK DIAGRAM AND OVERVIEW

The main part of this scheme consists of a DC-DC converter followed by a PWM inverter and a low-pass filter (LPF) as shown in Fig. 5.2.1.1.

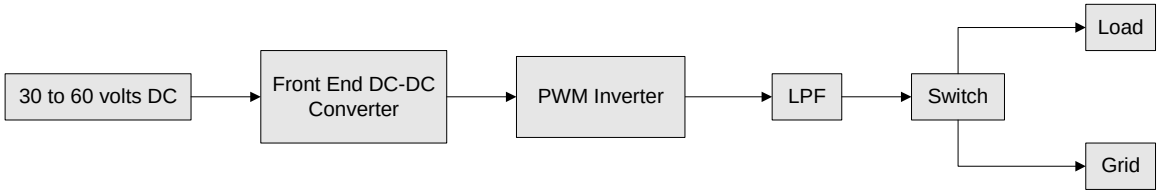


Fig. 5.2.1.1: A brief block diagram of the full system.

The input voltage (30~60 V DC) is fed to a DC-DC converter, involving an inverter, ferrite core transformer and full-bridge rectifier. The DC input voltage is switched at 25 KHz by a MOSFET bridge circuit to make a square wave. This square wave is stepped up by a ferrite core transformer to a level so that it can supply power at the required voltage even when the input voltage is the minimum (30V). The output of the transformer is then rectified and filtered with the help of ABS (absolute) circuit. Thus, we get a variable DC voltage at the converter's output. The variation of the output of the ABS circuit is due to the variation of input voltage source. It is fed to the PWM Inverter section.

The gate signal for the PWM inverter is generated off-line through the use of Look Up Table (LUT). Such a LUT, for operating at different output voltages, is saved into two EPROMs [2]. The second EPROM (EPROM2) stores the PWM pulse duties for various carrier cycles at a certain modulation index. And using that pulse duties, PWM patterns are generated through the data bus of first EPROM (EPROM1) as illustrated in Fig. 5.2.1.2:. A Demultiplexer is used here for sending PWM pulses to Q1, Q4 or Q2, Q3 at alternate half-cycles of the output waveform. When one of the above pairs is turned ON, the other is turned OFF. This results the waveform shown in Fig. 5.2.1.3 at the input of the filter.

A microcontroller selects the proper value of modulation index and hence selects the appropriate PWM pattern from the LUT, depending on the condition of grid voltages. Now for synchronizing the output AC voltage with the grid (in frequency and phase), we are using a PLL, involving Zero-Crossing Detector (ZCD), Phase Comparator, Low Pass Filter (LPF), Voltage Controlled Oscillator (VCO) and Counters (the same ones used in PWM pattern generation while off-line). So the synchronization with grid is automatic in our system, as long as the filter in the main part

ensures zero phase-shift. But in case of abnormal conditions in grid (under Voltage, over Voltage, frequency deviation out of predefined range, blackouts etc.), phase of the output voltage is synchronized with a pulse generated using a timer of the microcontroller. The microcontroller can easily detect the abnormal situation by sensing the grid condition and decide whether to be in grid or standalone mode. When in grid mode, the output frequency is synchronized with the grid frequency. In standalone, the frequency is set by the synchronizing pulse coming from the microcontroller.

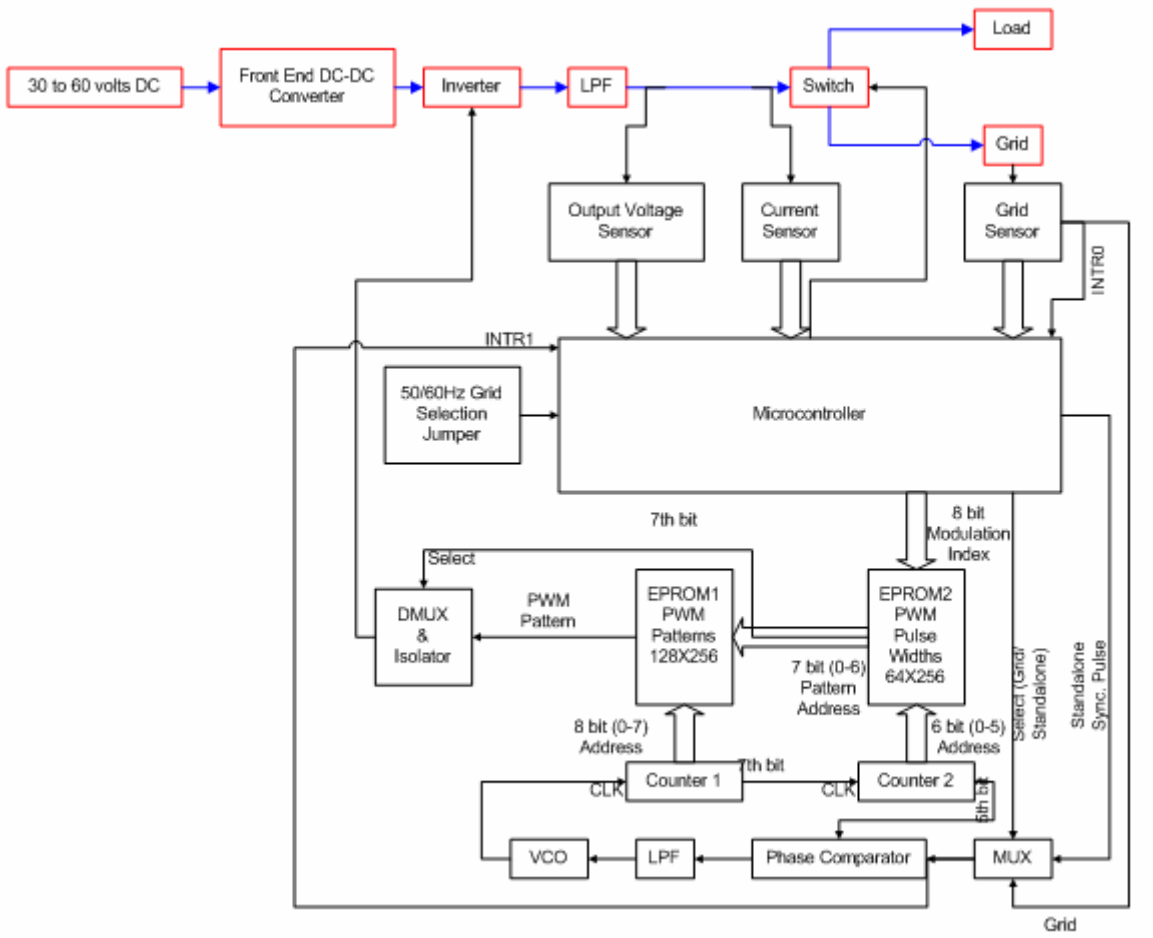


Fig. 5.2.1.2: Block Diagram representation of the final scheme [ZCD: Zero Crossing Detector, VCO: Voltage Controlled Oscillator, MUX: Multiplexer, DEMUX: Demultiplexer, LPF: Low-Pass Filter, PWM: Pulse Width Modulated]

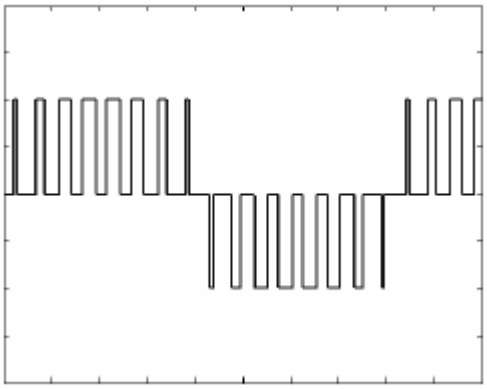


Fig. 5.2.1.3: Inverter's Output Voltage Waveform before filtering

After passing through the LC passive filter a sinusoidal waveform results, having very low distortion factor (DF). The filter is designed in such a manner so that it passes only the fundamental frequency, with very few harmonics and in the design it is also ensured that the phase shift between input and output of the filter at the fundamental frequency is negligible.

5.2.2 FRONT END DC-DC CONVERTER

In the DC-DC converter section, a conventional configuration (Fig. 5.2.2.1), involving an input filter, a switching bridge, a ferrite core transformer, a bridge rectifier and an output filter, is used. The input dc, after passing through a low-pass filter is fed to the switching bridge circuit. The output of the switching bridge is an ac square wave of 30-60V peak which is then supplied to the primary of the ferrite core transformer. The turns ratio of the transformer is so designed that the output peak voltage corresponding to 30V peak is 400V. To reduce the transformer size, the input dc voltage is first converted to high frequency square ac (25 KHz) and is then stepped up with the help of ferrite core transformer. The secondary voltage of the transformer is rectified and filtered with the help of ABS (absolute) circuit. The output of the DC-DC converter (output of the filter section) is fed to the inverter.

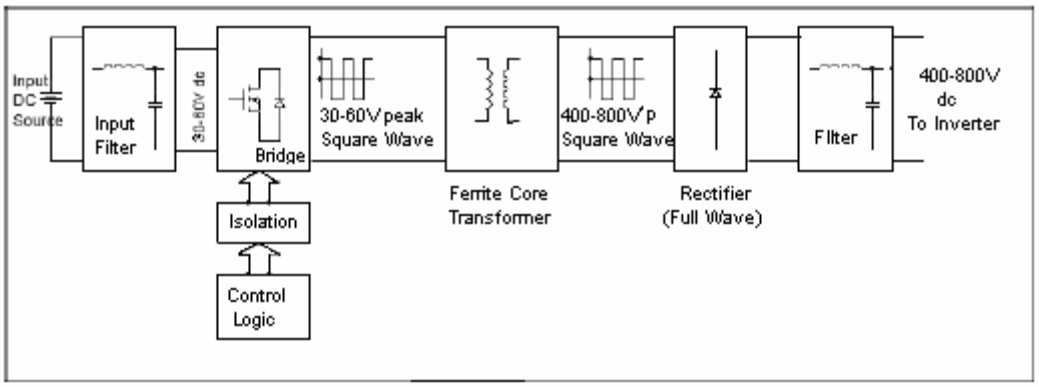


Fig. 5.2.2.1: Block diagram of front end dc-dc converter.

5.2.2.1 DESIGN

The front dc-dc converter involves an input low-pass filter, a switching bridge, a ferrite core transformer, a rectifier bridge and an output low-pass filter. The targeted efficiency of dc-dc converter was 91% and the targeted overall efficiency was 90%. The following criteria were followed.

Maximum input power to the dc-dc converter, P_{dc}: ***1kW/0.90 = 1.1kW***
Input voltage, V_{in}: ***30 ~ 60V***
Output voltage, V_s : ***400~800V***
Switching frequency, f_s : ***25kHz***
Transformer turns ratio, $N_p : N_s$ = ***1 : 13.3***
Targeted efficiency η = ***91%***

5.2.2.2 SWITCH DESIGN

The bridge network contains four switches. BUET team used four MOSFETs to implement the switches.

Minimum input voltage to the bridge, $V_{in\text{-}min}$ = ***30V***

Maximum input voltage to the bridge, $V_{in\text{-}max} = 60V$

Maximum switching current $I_{d\text{-}max} = 1.1kW/30 = 36.67A$

Targeted efficiency $\eta = 95\%$

Maximum average switching loss (per switch) $P_{sw\text{-}loss} = 27.5W$

Maximum ON resistance, $r_{ds(on)} = P_{sw\text{-}loss} / I^2_{dc\text{-}max} = 20.5m\Omega$

For safety of operation and cost-efficiency trade off the MOSFETs of ***100V, 40A, 50mΩ*** were selected. **IRF 150** covers the requirements [5]. So **IRF 150** was selected.

5.2.2.3 TRANSFORMER DESIGN

The ferrite core transformer used in the converter was designed, taking reference from [3]. Core size and required number of turns in primary and secondary winding are calculated as given below. The targeted efficiency of the transformer is 96%.

5.2.2.3.1 CORE SIZE

The power handling capacity of a transformer core is determined by its area product Wa , where W is the available core window area, and a is the effective core cross-sectional area.

$$Wa = \frac{P_{dc} S.10^8}{4eBfk}$$

Where, P_{dc} is output power, S is current density, e is transformer efficiency, B is flux density, f is switching frequency and K is winding factor. For our core, Wa was calculated to be 80 cm^2.

5.2.2.3.2 NUMBER OF TURNS

The number of turns is calculated using:

$$\frac{N}{V} = \frac{10^8}{28.64\, faB}$$

Where,

f = Frequency of operation of the transformer (20KHz in our case)

a = Core cross section area, 1.24in^2

B = Flux density in the core, 1Kgauss

The maximum primary voltage in our case is 60V, which requires primary turns of 8.46. And we have taken 10 turns, considering some safety margins. Now, for obtaining a 240V AC using a minimum of 30V DC, we need to provide at least 400V DC at the inverter bus. So, the required turns ratio is 400/30 = 13.33. Hence, turns required in the secondary coil are 13.33x10 = 133.3. And considering some safety margin, we have used 135 turns.

5.2.2.3.3 CONDUCTOR SELECTION

The rms value of the winding current determines the wire size of the winding. The maximum rms value of the primary and secondary winding was calculated respectively 35A and 6A. We used **sheet** of copper capable of carrying the required current for our primary turns and round wire of 16 AWG for secondary turns.

5.2.2.4 BRIDGE RECTIFIER DESIGN

The high frequency ac square wave is fed to the bridge rectifier. The diodes of the rectifier were selected using following criteria.

Input voltage, V_s ***: 400~800V(peak)***

Targeted efficiency, η ***= 99.5%***

Maximum input power to the bridge, P_{ac}***: 1.1kWx0.95 = 1.045kW***

Maximum diode current, $I_{d\text{-}max}$ ***= 2.61A***

Maximum average conducting loss (per diode), $P_{c\text{-}loss}$ ***= 2.61W***

Forward Voltage, V_F ***= 1V***

Peak reverse voltage, V_{pr} ***= 900V***

AC frequency, f_s ***: 25 kHz***

Reverse recovery time, t_{rr} ***: 400 ns***

For design safety BUET team chose V_{pr} ***=1000V,*** I_F***=5A,*** V_F***=1.0V,*** t_{rr}***=200ns***. **BY329X** from Philips Semiconductors fulfils the requirement [5] and hence was chosen.

5.2.2.5 FILTER DESIGN

After the bridge rectifier a low-pass filter is used to produce a low ripple dc voltage. The frequency of the ac signal is ***25 kHz***. Hence, the output of the bridge rectifier will contain fundamental and the higher harmonics of ***25 kHz***. Thus a LC filter of ***10 kHz*** cut-off frequency would be enough. BUET team chose ***C = 330μF, L = 2μH.***

5.2.3 PWM INVERTER

The input to the device (Utility Interactive Inverter System) is a variable 30-60V dc. BUET team here used a dc-dc converter to raise the dc level. Hence the output of the dc-dc converter will vary with the variation of the input. The output of the device (Utility Interactive Inverter System) is a sinusoidal voltage that will be used to feed a resistive load at standalone mode and to supply power to the grid when it is connected to the grid. To synchronize with the grid, amplitude, frequency and phase of the output sinusoidal wave must be equal to those of the grid. Moreover, amplitude and frequency of the grid may vary within a certain limit described at RFP (Request For Proposal) of IFEC2005. So, in this stage we needed an inverter that is capable of giving a

sinusoidal voltage output whose amplitude, frequency and phase are exactly equal to the amplitude, frequency and phase of the grid voltage respectively. And if the grid voltage and frequency changes within the allowable limit, the inverter will keep track with the change to be synchronized with the grid.

To fulfill the above requirements BUET team chose the PWM Inverter where the PWM patterns are calculated offline using very high speed microcomputer and is stored to EPROMs as described in [2]. And the EPROM is used as LUT for a very cheap microcontroller. Hence, the low cost microcontroller makes decision about the selection of proper PWM pattern for a desired output voltage. However, there are some differences between the technique described in [2] and the one BUET team used here.

5.2.3.1 ANALYSIS OF REGULAR SAMPLED PWM

Analog PWM control is accomplished by employing the natural sampling strategy. The basic circuit uses a comparator to detect the intersection of the triangular (carrier) wave with a sinusoidal modulating wave. The resultant output is a periodic pulse train that switches at points determined by the relative magnitude and frequency of its two inputs. Since the switching edge of the width-modulated pulse is determined by the instantaneous intersection of the two waves, the resultant pulse width is proportional to the amplitude of the modulating wave at the instant where the switching occurs. This natural sampling process is therefore real-time in nature providing instantaneous response to demand variations, such as a change in amplitude of the modulating wave, but there is minimal choice strategy. This has two important consequences: (i) the centers of the pulses in the resultant PWM wave are not equidistant, or uniformly spaced; (ii) it is not possible to define the width of the pulses using analytic expressions. Hence analog PWM control is not suitable for our scheme.

In regular sampled PWM, the modulating sine wave is regularly sampled. This can be visualized as shown in Fig. 5.2.3.1.1 for symmetric regular sampled double edge PWM. Now it is informative to consider regular sampling as a digital process of sampling a sinusoidal modulating wave (a) at regularly spaced intervals to produce sinusoidal weighted digital samples of the modulating wave, as presented by (b) in Fig. 5.2.3.1.1.

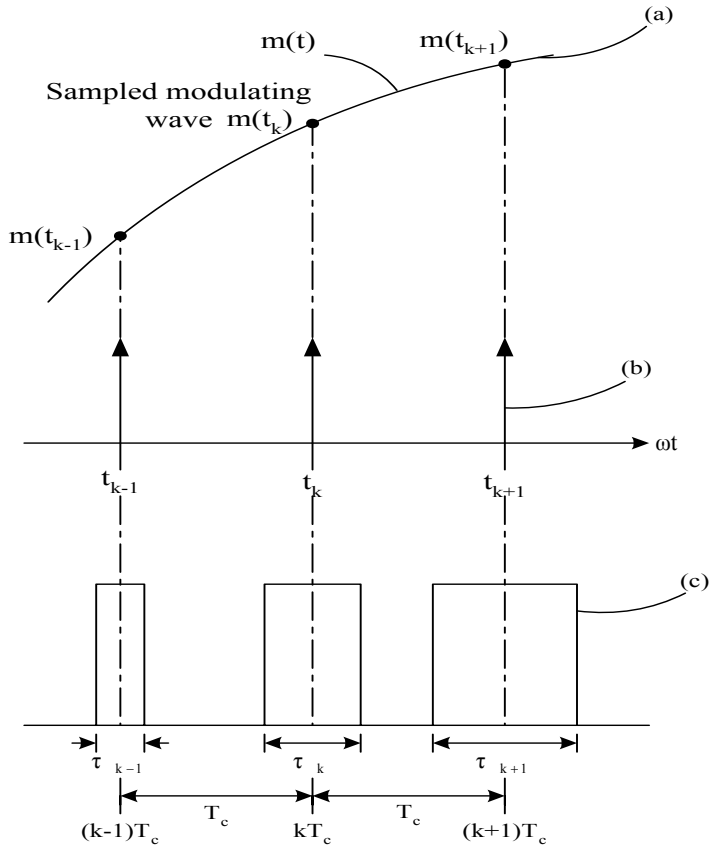


Fig. 5.2.3.1.1: Regular Sampled symmetric double edge modulation (a) Modulating waveform (b) Regular-Sampled waveform (c) PWM waveform

As shown in Fig. 5.2.3.1.1, the process consists of taking samples $m(t_k)$ of a modulating wave $m(t)$ at regularly spaced time intervals $t_k = kT_c$, where T_c corresponds to the sampling period. These samples of the modulating wave $m(t_k)$ are subsequently used to modulate the width, τ_k, of the PWM waveform such that the pulse width (τ_k) is proportional to $\sin(\omega t_k)$ (for sinusoidal modulation), resulting in each edge of the pulse modulated equally. For computations of switching points/pulse widths, the reference sine waveform is approximated to a stepped sine wave. With this approximation, there exist defined equations for computation of the switching points of the PWM control pattern, which is done in the following section.

5.2.3.2 DETERMINATION OF PWM PULSE WIDTHS AND SWITCHING POINTS

As stated earlier, in the regular sampled PWM (RSPWM), the modulating sine wave is regularly sampled and the PWM pulse widths are calculated on carrier cycle basis. The triangular carrier wave determines the sampling points. The sample of sine wave is taken at every zero point of the triangular carrier wave and is assumed to be constant over the carrier period as depicted in Fig. 5.2.3.2.1.

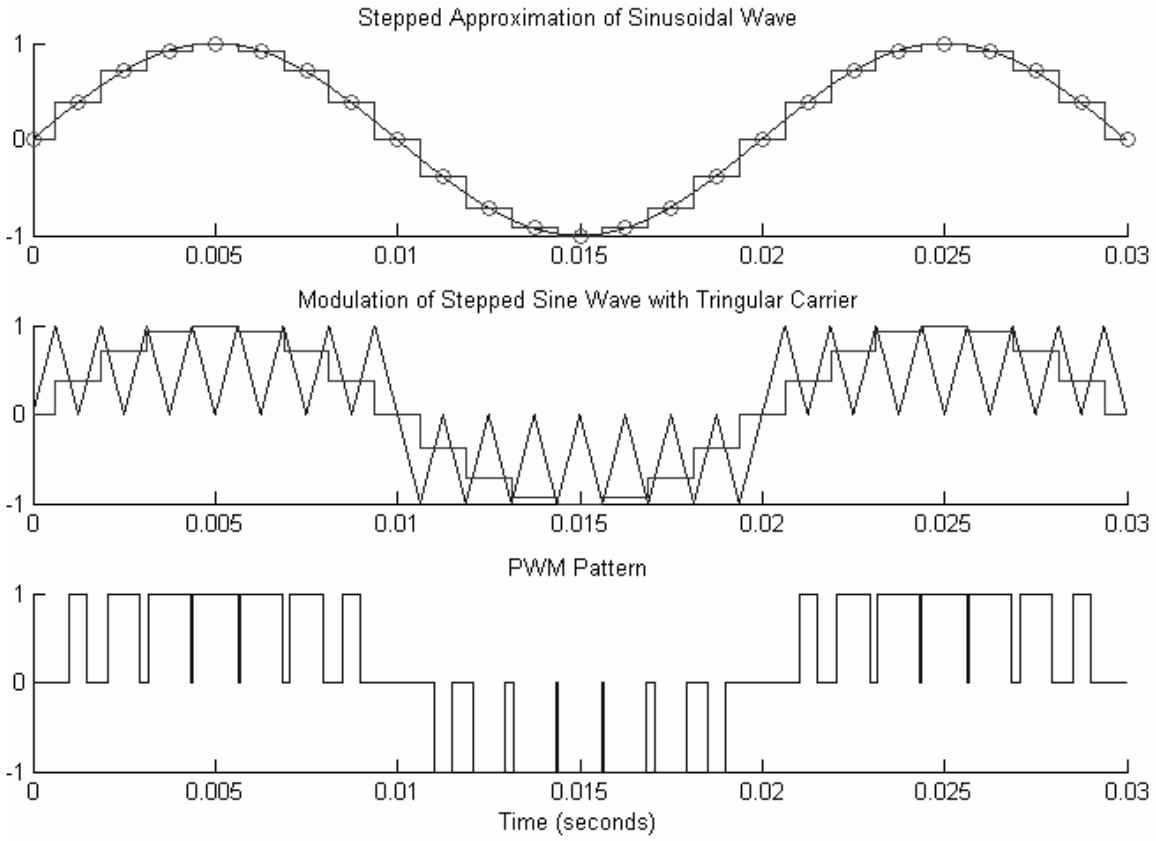


Fig. 5.2.3.2.1: (a) Stepped approximation of sine wave. (b) Modulation of stepped sine wave with triangular carrier. (c) PWM pattern.

Since the samples are taken at every zero point of the carrier wave, the lengths of the steps of the stepped wave are equal. The amplitude of the reference sine wave modulates the width of the pulses. To do this the stepped sine wave is compared with the carrier wave. Since the magnitude of the stepped sine wave is constant within a carrier period, the PWM pulses are symmetrical about sampling point as shown in Fig. 5.2.3.2.2.

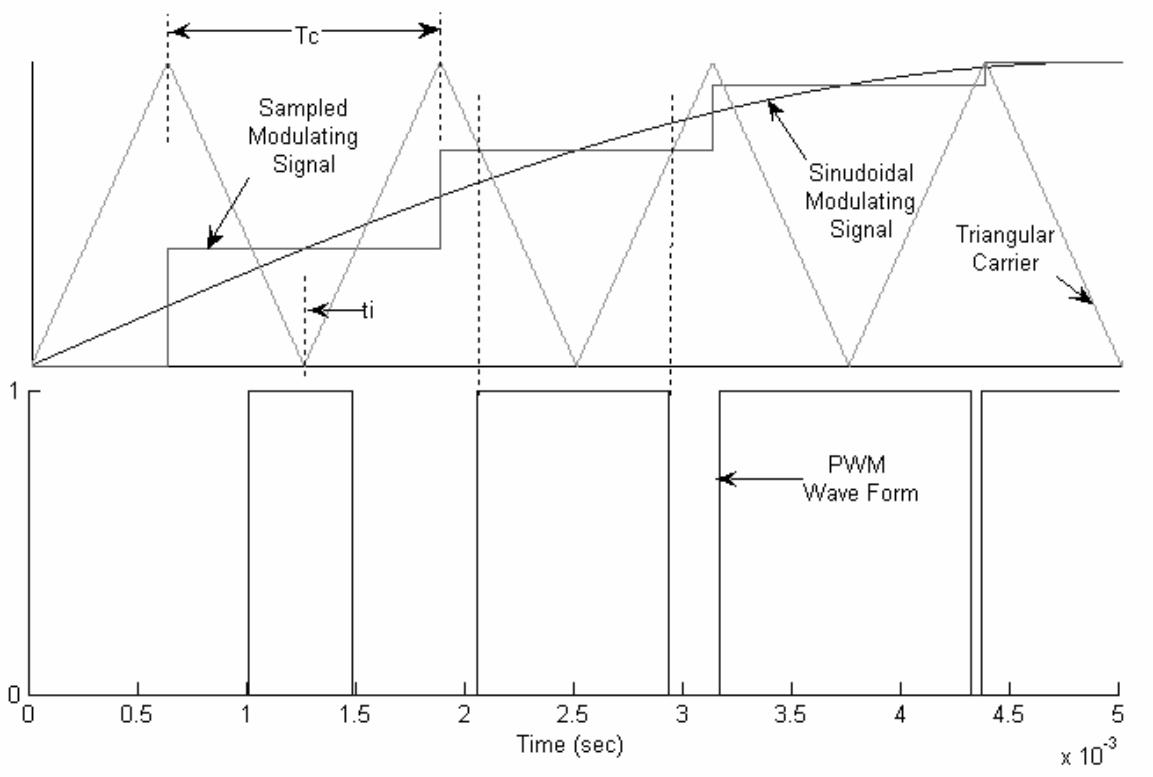


Fig. 5.2.3.2.2: Regular Sampled Symmetric PWM obtained from comparison of the stepped sine wave reference with a triangular carrier wave.

The harmonic spectrum of RSPWM contains the fundamental, and the harmonics up to the carrier frequency are negligible by the nature of the modulation process. The amplitude of the fundamental is determined by the modulation index, *M*. The modulation index *M* is defined as $M = V_m/V_s$, where, V_m is the peak value of the modulating sinusoid and V_s is the supply voltage of the inverter.

As mentioned earlier, the RSPWM pulses are regularly spaced and symmetrical about its sampled time. Thus a mathematical expression can easily be developed for the pulse width of the PWM pulses inspecting geometry of the waveforms as depicted in Fig. 5.2.3.2.3.

Let us consider following sinusoidal wave having amplitude A_m and angular frequency ω as the modulating signal,

$$f(t) = A_m \sin \omega t \qquad (5.1)$$

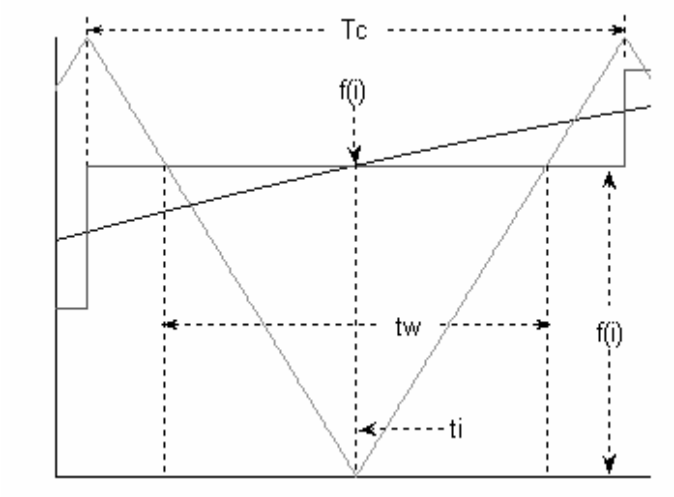


Fig. 5.2.3.2.3: A complete carrier cycle showing the geometry of the carrier, approximated stepped sinusoidal and modulating waves.

As shown in Fig. 5.2.3.2.1 samples are taken at every zero point of the carrier triangular wave. If N_c samples are taken at every period of the modulating signal, the magnitude of the i^{th} sample may be determined by,

$$f(i) = A_m \sin\left\{\frac{2\pi}{\mathrm{N_c}}(i-1)\right\} \tag{5.2}$$

To approximate the modulating sinusoidal as a stepped sinusoidal the sampled voltage is assumed to be constant over the carrier cycle.

In Fig. 5.2.3.2.3 complete carrier cycle is shown. Here sample of the sinusoidal is taken at $t = t_i$. The magnitude of the sine wave is assumed to be constant over carrier period (T_c) and is compared with the magnitude of the triangular carrier wave (of amplitude A_c) to produce the PWM pulse. The width of pulse t_w depends on the value of sampled sinusoidal *f(i)*. The width of the pulse is given by,

$$t_w(i) = T_c \frac{A_m}{A_c} \sin\left\{\frac{2\pi}{\mathrm{N_c}}(i-1)\right\} \tag{5.3}$$

$$\text{or, } t_w(i) = T_c M \sin\left\{\frac{2\pi}{\mathrm{N_c}}(i-1)\right\} \tag{5.4}$$

Where, $M = \frac{A_m}{A_c}$ is called Modulation Index. As shown in Fig. 5.2.3.2.1(c), the output of the inverter contains three voltage levels $+V_s$, *0* and $-V_s$. For the *i*-th carrier-period, the output voltage of the inverter is either $+V_s$ or $-V_s$ for time t_w and zero for T_c - t_w. The average (dc) value of the PWM pulse for the *i*-th carrier-period is equal to the instantaneous amplitude of the output stepped fundamental voltage, $v(i) = V_m \sin\left\{\frac{2\pi}{\mathrm{N_c}}(i-1)\right\}$. The average value of the PWM output voltage over one complete carrier cycle is thus given by,

$$V_m \sin\left\{\frac{2\pi}{\mathrm{N_c}}(i-1)\right\} = \frac{t_w(i)V_s - 0}{T_c}$$

or,

$$t_w(i) = T_c \frac{V_m}{V_s} \sin\left\{\frac{2\pi}{\mathrm{N_c}}(i-1)\right\} \qquad (5.5)$$

It is obvious that equation (5.3) and (5.5) are similar. Hence from (5.3) and (5.5), we get $M = \frac{V_m}{V_s}$. So, it can be written that, $M = \frac{A_m}{A_c} = \frac{V_m}{V_s}$. Hence equation (5.5) can be written as,

$$t_w(i) = T_c M \sin\left\{\frac{2\pi}{\mathrm{N_c}}(i-1)\right\} \qquad (5.6)$$

From the above equation, we find that pulse width t_w is a function of sampling interval or carrier period (T_c), number of samples per fundamental period (N_c), modulation index (M) and the sample number (i). Sampling interval inversely varies with the carrier frequency. Hence, we can control the width of PWM pulses by varying the modulation index, the carrier frequency and the modulating signal frequency.

From equation 5.6 it is evident that the calculations of PWM pulse widths involve floating point operations. Normal microprocessors do not possess built-in math coprocessor and cannot perform floating-point calculations. These processors are designed to perform integer type multiplications, divisions, additions, subtractions etc. MMX processors have built-in math coprocessor, which can perform floating-point calculations. However, it will not be cost effective to use MMX processor for the real time implementation of PWM scheme. For this reason, the simplified version of the

above equation is used where the data i.e. modulation indices (*M*) and sine values are of integer type so that the scheme can be implemented using low cost processor.

Now, let the total number of samples in a carrier period = *R*. Hence, the duration of each sample is given by,

$$\Delta t = \frac{T_c}{\mathrm{R}}.$$

Now, PWM pulse width is given by,

$$t_w(i) = \Delta t K_w(i)$$

Where, K_w is called pulse width tag which is in the scale of R. Equation 5.6 can be written as,

$$K_w(i) = RM \sin\left\{\frac{2\pi}{\mathrm{N_c}}(i-1)\right\}$$

Again Modulation index can be normalized to a scale of R. Modulation index M can be written as, $M = M_o + \Delta M K_m$ where, $\Delta M = \frac{M_{\max} - M_o}{\mathrm{R}}$ and K_m is an integer. When $K_m=0$, $M=M_o$ and when $K_m = R$, $M=M_{max}$. Hence modulation index can be varied by varying modulation index tag K_m.

Equation 5.6 is now changed to,

$$K_w(i) = R\left[M_o + \Delta M K_m\right]\sin\left\{\frac{2\pi}{\mathrm{N_c}}(i-1)\right\} \qquad (5.7)$$

With the help of equation 5.7 for a given normalized modulation index tag K_m, widths of PWM pulses can be calculated in the scale of R using a MMX microprocessor. It should be noted that, $K_w < R$ and $K_m < R$. Thus if *R* is chosen to be 256, then value of K_w and K_m will lie between 0 and 256. Since the values of K_w and K_m are less than 256, the values of K_w can be stored in an EPROM and an 8-bit microprocessor can be used to select proper modulation index tag to produce required PWM pulses for desired output voltage.

BUET team developed MATLAB programs to calculate the PWM pulse patterns for different modulation index.

5.2.3.3 IMPLEMENTATION OF PWM INVERTER

The PWM inverter consists of a microcontroller module board, bridge switch and a low-pass filter. The microcontroller module board contains the PWM pulse generator and voltage and current sensors. In this section the detailed description and design of the PWM inverter will be given.

5.2.3.3.1 PWM GENERATOR SCHEME

Fig. 5.2.3.3.1 shows the PWM gate pulse generator scheme. In this scheme, PWM pulse width is calculated offline by a high speed microcomputer (MMX microprocessor). There are two EPROMs. EPROM1 contains pulses of 128 different duty cycles (0% to 100%). Each pulse consists of 256 bits. Hence, a pulse of 50% duty cycle consists of 64 zeros, 128 ones and 64 zeroes consecutively. In a fundamental period there are 64 PWM pulses for a given modulation index. The widths of these PWM pulses are calculated offline and stored in EPROM2. Every pulse width is 7 bits (0-6) long and is used to address the EPROM1. The 7^{th} bit of EPROM2 is used as the selection pin of the de-multiplexer that is used to de-multiplex the PWM patterns to the gates. The Counter1, Counter2, Phase Comparator, LPF and a VCO comprise the phase locked loop which is used to synchronize the phase and frequency of the output of the inverter to the phase and frequency of the grid voltage when connected to the grid, and when inverter is in stand alone mode, the synchronization pulse (50/60Hz) is provided from the microcontroller. Counter1 provides lower 8bit addresses for EPROM1. And upper 7 bit address is provided by EPROM2. Counter2 provides lower 6 bit address, and upper 8 bit address is provided from the microcontroller as Modulation Index. For a fixed modulation index, when Counter2 counts 0, 1, 2, … 63, the output of EPROM2 is the widths of 1^{st},2^{nd}, 3^{rd},….64^{th} pulses of PWM pattern for that modulation index respectively. These pulse widths are used to select the appropriate pattern from EPROM1 to generate the gate pulses of MOSFET. The 7^{th} bit of EPROM2 is used to specify the sign of PWM pulses and hence the 7^{th} bit determines either transistor Q1 and Q4 or transistor Q2 and Q3 should be turned on.

The scheme described above is used very effectively to synchronize the inverter to the grid. The PLL part of the scheme ensures the matching of frequency and phase of output voltage with the frequency and phase of the grid voltage even if the frequency of the grid varies within the limit. And the matching of the third parameter of synchronization, namely, the amplitude of the voltage is done by changing the modulation index.

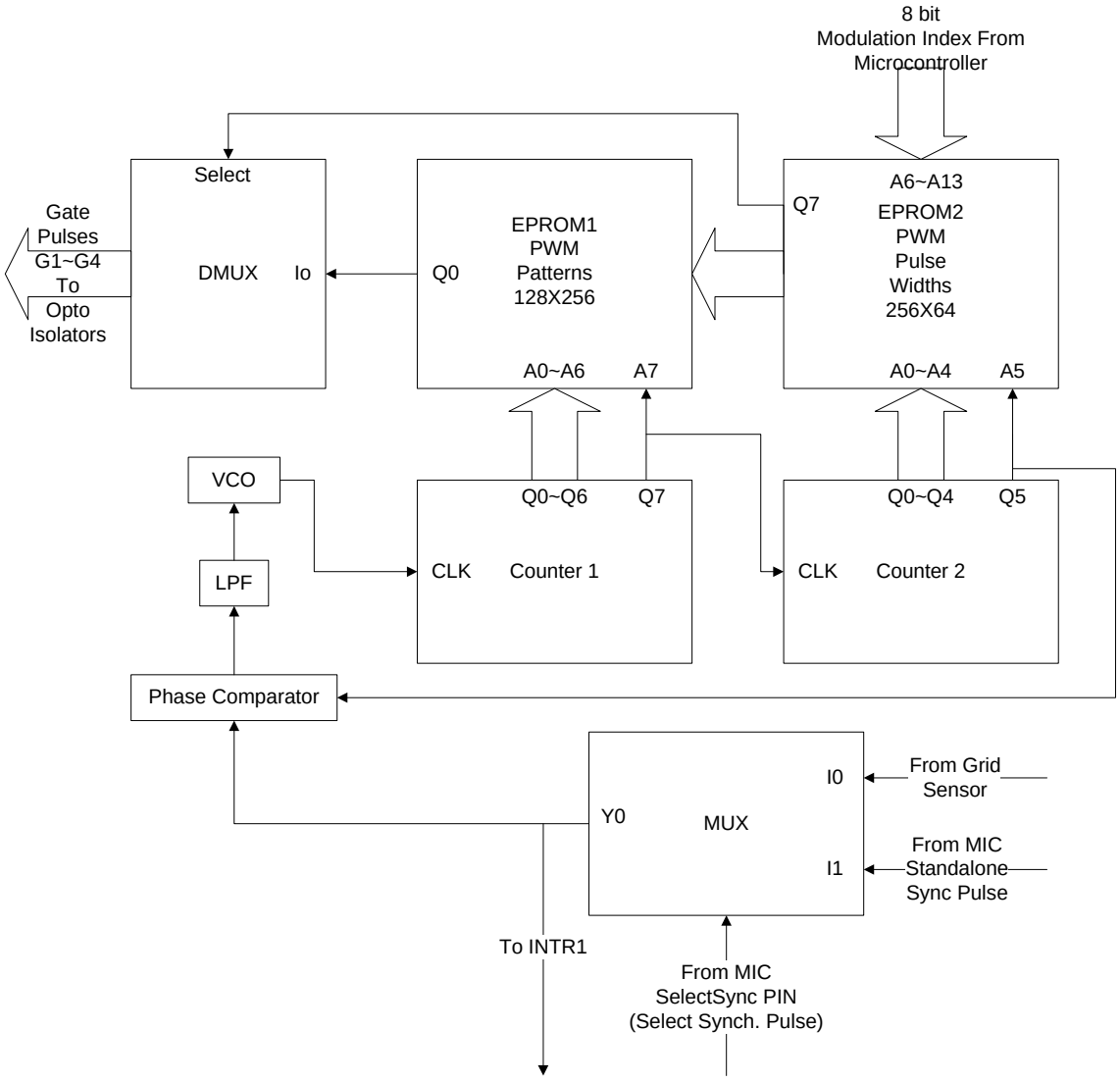


Fig. 5.2.3.3.1: PWM gate pulse generator scheme.

5.2.3.3.2 DESIGN

The distortion factor and the harmonic profile of the PWM inverter system depends on the carrier frequency of the modulation. The design criteria are given below:

PWM carrier, f_c***=3.2 kHz (50Hz/240V grid), 3.84 kHz (60Hz/110V grid)***
Number of pulses per fundamental period, N_c***=64***
Resolution, ***R=256 (8-bit)***

Microprocessor: ***8-bit, 12MHz.***
Memory:
RAM: ***256 byte***
ROM: ***48kByte, EPROM***

To meet the criteria BUET team selected an **8-bit** microcontroller with **256** bytes of SRAM **8kByte** flash program memory and **48kByte** of EPROM. **AT89C52** (microcontroller from ATMEL) is selected [5].

5.2.3.3.3 MICROCONTROLLER MODULE BOARD

The microcontroller board controls the operation of the whole Inverter scheme. The functional blocks of the module of the microcontroller, is shown in Fig 5.2.3.3.3. It is equipped with a low cost AT89C52 microcontroller, four 8-bit latches and an 8-bit A/D converter (ADC0808), capable of converting data coming through 8 channels (Only three channels are used in our scheme for sensing grid voltage, output voltage and output current). The AT89C52 microcontroller from Atmel has internal 8K flash EEPROM, 256 byte SRAM, 4 ports and 3 programmable timers (2 of them were used) and is suitable for implementing such interactive inverter scheme with minimal hardware. As mentioned earlier, the microcontroller chooses the value of modulation index for the first stage EPROM. Moreover, two of the timers are used in the scheme, one for measuring grid frequency and one for providing synchronization pulse when the system is in standalone

mode. The 50/60 Hz selector switch selects whether the system should operate in 110V (60Hz) or in 240V (50Hz).

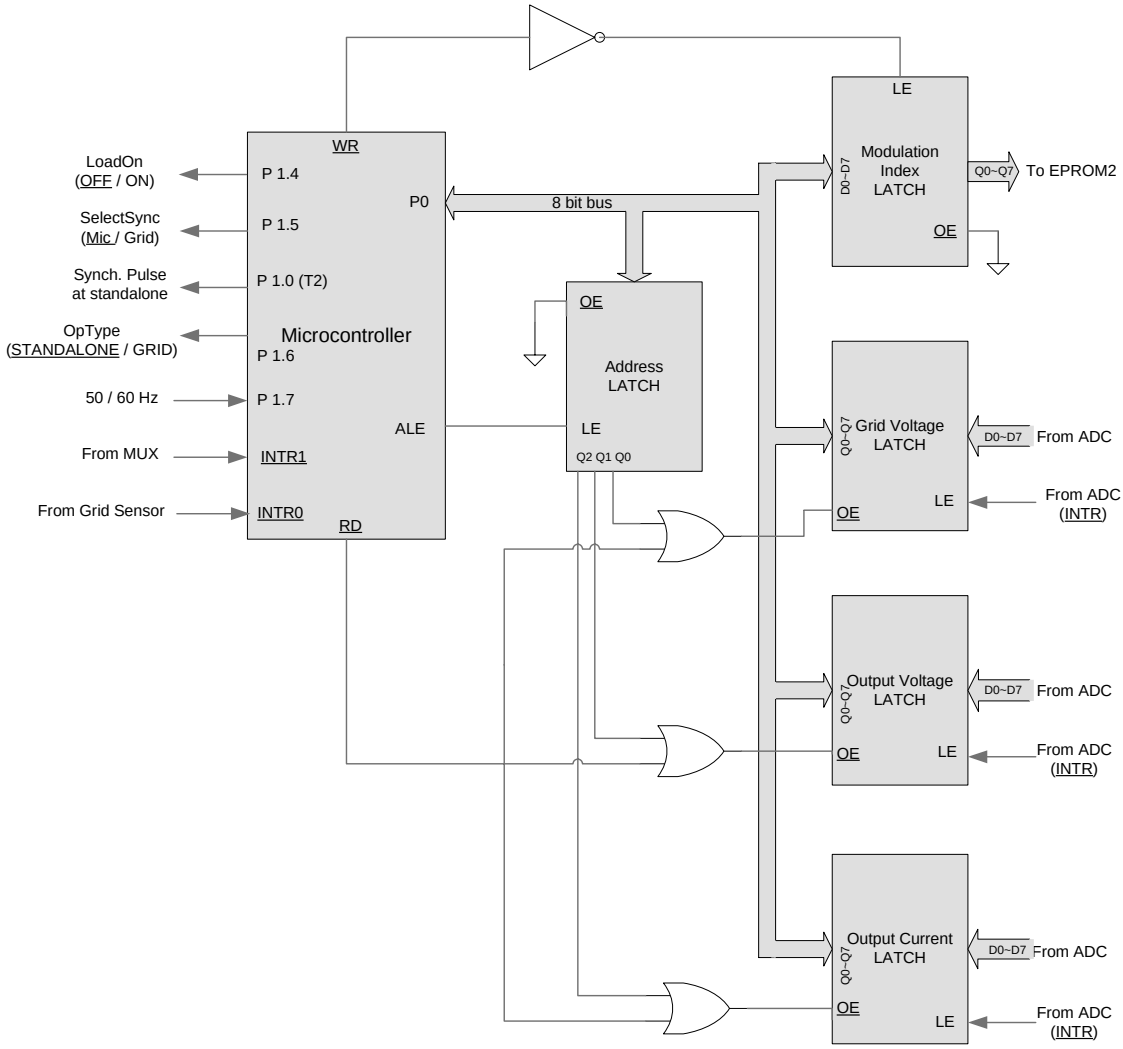


Fig 5.2.3.3.3: Microcontroller Module Board.

5.2.3.3.4 CONTROL ALGORITHM USING MICROCONTROLLER

In the main routine of our algorithm, different values are initialized for two different grid conditions (*110V, 60Hz* and *240V, 50Hz*) and the program waits for any of the two interrupt signals at the interrupt pin of the microcontroller. Since the microcontroller is 8 bit, all the voltages are normalized to fit in 8 bits. BUET team assumed that, maximum and minimum

peak voltages are to be handled by the microcontroller are 450V (peak) and 110V (peak) respectively. The normalized voltage is given by the equation,

$$V_{normalized} = \frac{V_{actual} - V_{\min}}{\Delta V}$$

Where, $\Delta V = \frac{V_{\max} - V_{\min}}{256}$

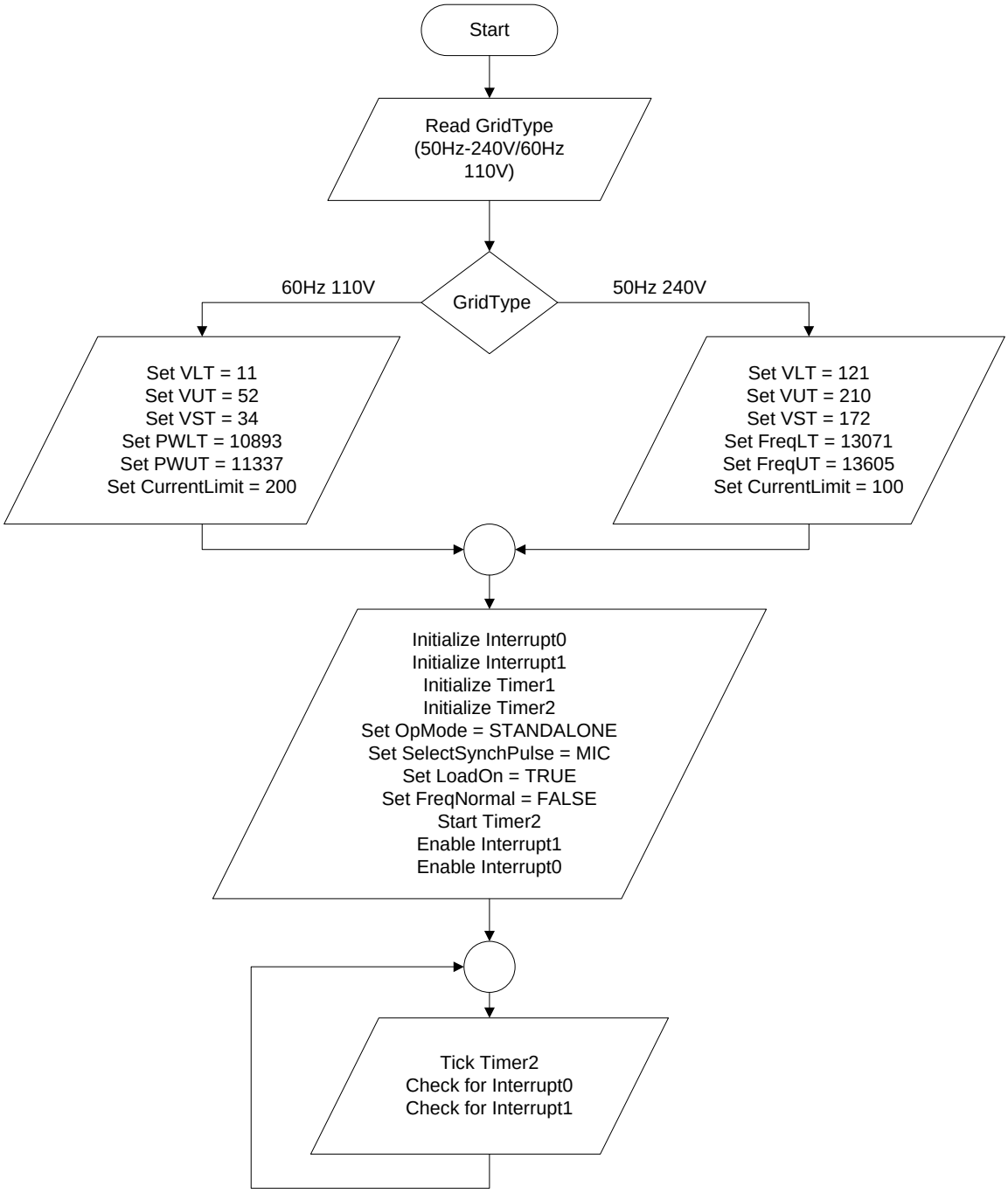


Fig. 5.2.3.3.4: Main Routine [LT: Lower limit, UT: Upper limit, PW: Pulse Width], All voltage limits are normalized.

The algorithms are implemented in C programming language and are compiled for AT89C52 microcontroller. The main algorithm is shown in Fig. 5.2.3.3.4.

5.2.3.3.5 INTERRUPT0 SUBROUTINE

In this subroutine, the frequency of the grid signal is measured using Timer 1 of the microcontroller and checked whether it is within 2% of the set value (50/60 Hz).

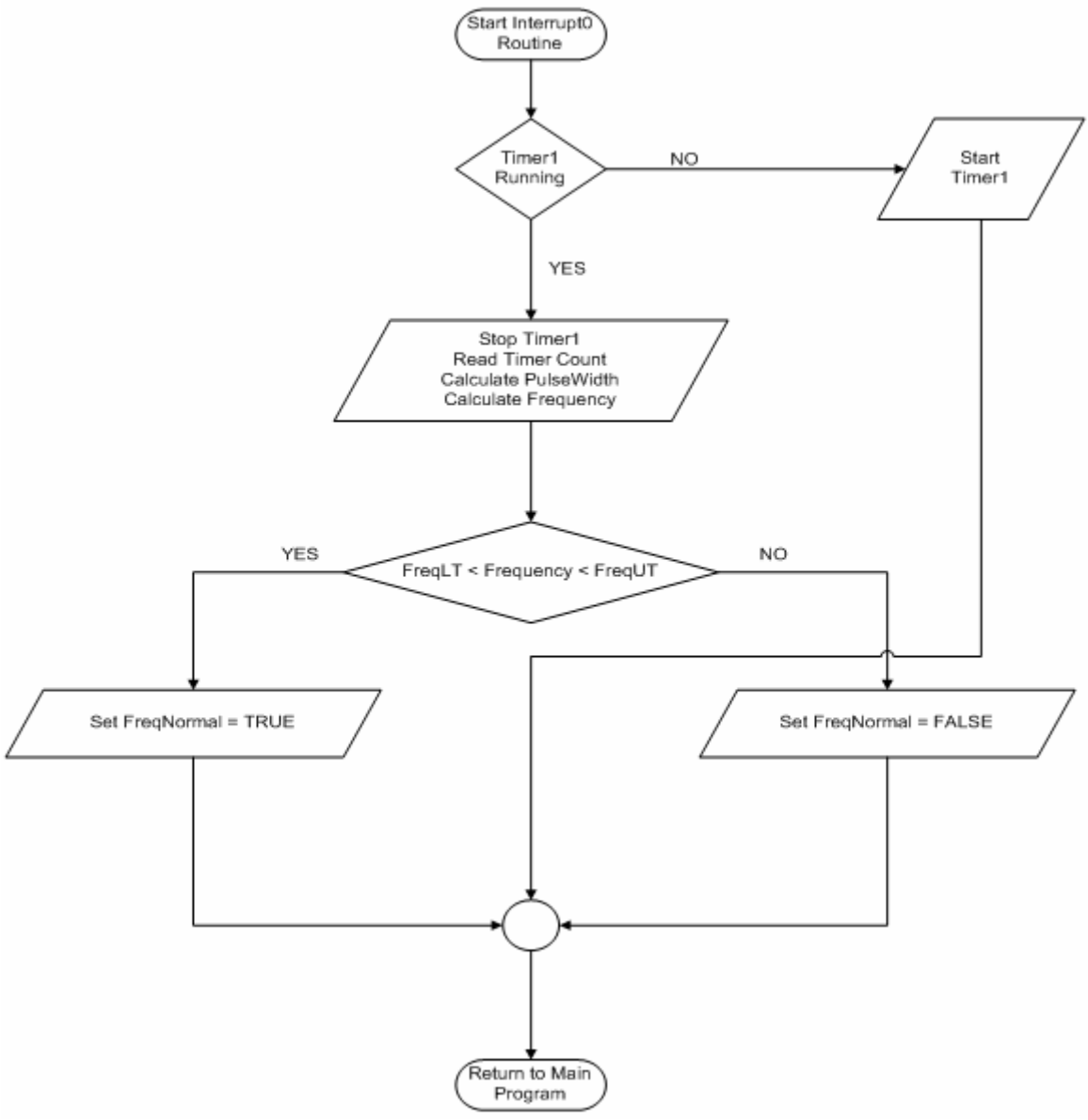


Fig. 5.2.3.3.5: Interrupt0 Subroutine [LT: Lower limit, UT: Upper limit]

Depending on the status of the grid frequency, abnormal condition is determined and certain measures are taken in Interrupt1 subroutine. Interrupt0 is called at every positive going zero crossing of the grid voltage. Hence, frequency of the grid is determined once at every two periods of grid sinusoid. Thus the inverter system is capable of detecting any abnormal frequency condition within two fundamental cycles of grid voltage. Fig. 5.2.3.3.5 is the graphical representation of the algorithm.

5.2.3.3.6 INTERRUPT1 SUBROUTINE

In this part of the program, all the output signals are generated for obtaining desired AC signal at the desired frequency as shown in Fig. 5.2.3.3.6. The selection of operation between Grid/Standalone is also done here. If the frequency and voltage are within some set limits, then grid operation is performed and the voltage is set to the grid value by changing the modulation index. But if either the frequency or voltage limit is crossed, then the system switches to Standalone mode, driving a *250W* resistive load and generating the standard grid voltage (*240V/50Hz* or *110V/60Hz*) at its output. In this condition, the synchronization pulse, which was extracted from grid in Grid mode, is generated by using Timer 2 of the microcontroller. The output current is also sensed by using a Current Transformer and checked whether desired output power is being provided and whether any abnormal situation present there.

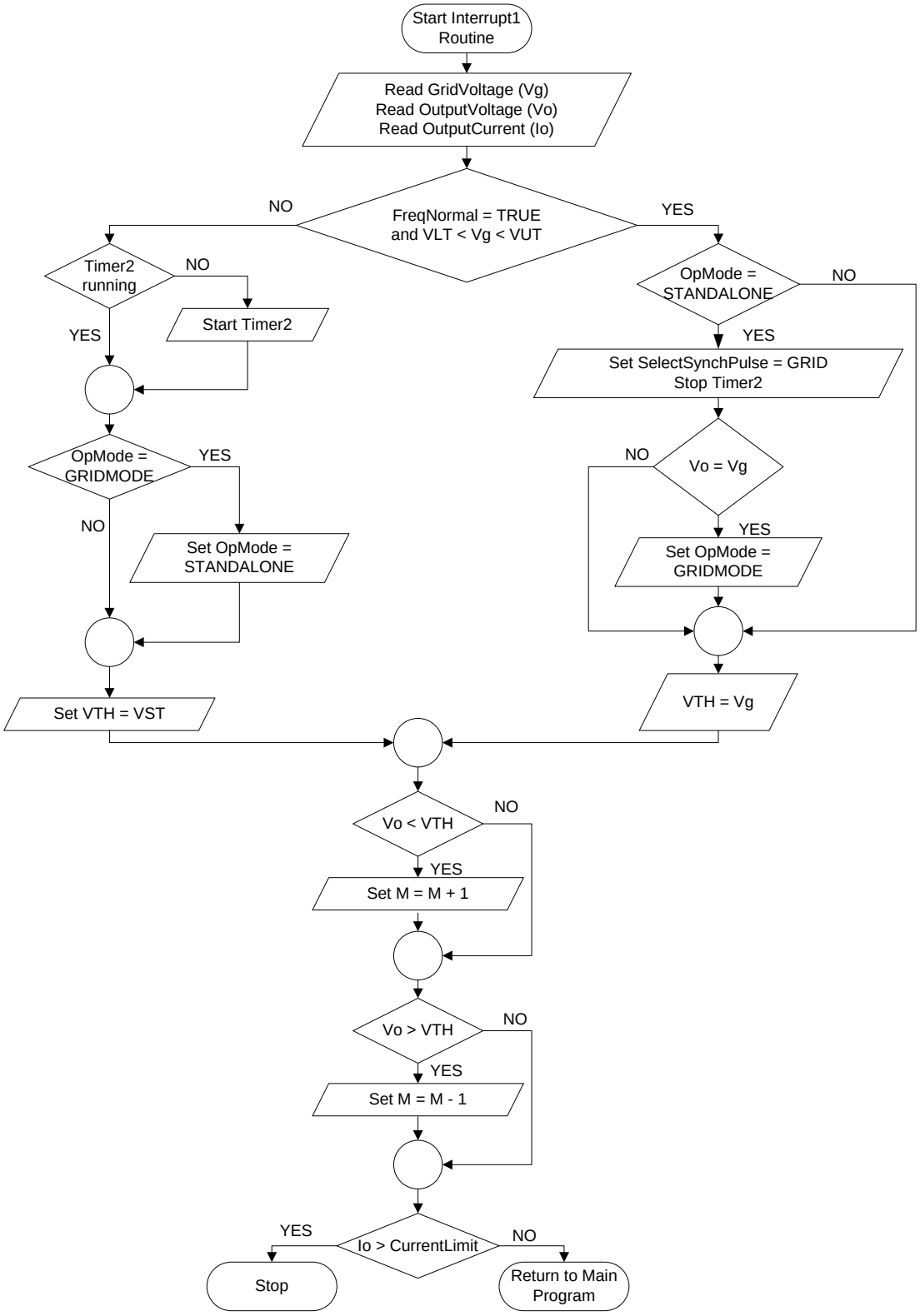


Fig. 5.2.3.3.6: Interrupt1 Subroutine [LT: Lower limit, UT: Upper limit, M: Modulation index, Vg: Grid voltage, VST: Voltage required at standalone, Vo: Output voltage, VTH: Voltage to be achieved before turning ON the synchronization switch, Io: Output Current]

5.2.3.3.7 VOLTAGE SENSOR

The voltage sensor circuit is presented in Fig. 5.2.3.3.7. It is a standard one consisting of a Potential Transformer (PT), buffer and a sampler. The potential transformer (PT) scales down the ac voltage level to a measurable value. The secondary voltage is fed to the buffer. The output of the buffer is fed to the sample and hold circuit. The sampler circuit samples the peak voltage and the ADC is triggered exactly at the positive peak of the input sinusoid. The exact triggering is done with the help of the 90^o phase shifter, zero crossing detector and the falling and rising edge detector. The sampler circuit is then reset at the negative peak of the input sinusoid. On completion of conversion ADC latches the digital value to the D Latch with the help of the interrupt signal. Hence the peak voltage of the input ac signal is sensed and stored in the memory circuit. Similar configurations were used for measuring output current, where the PT is replaced with a Current Transformer (CT).

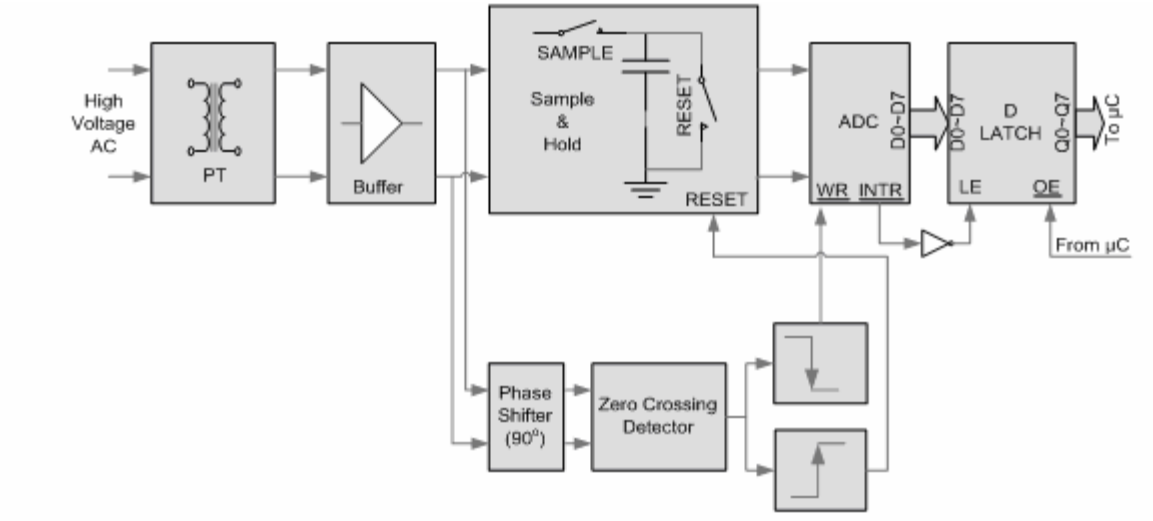
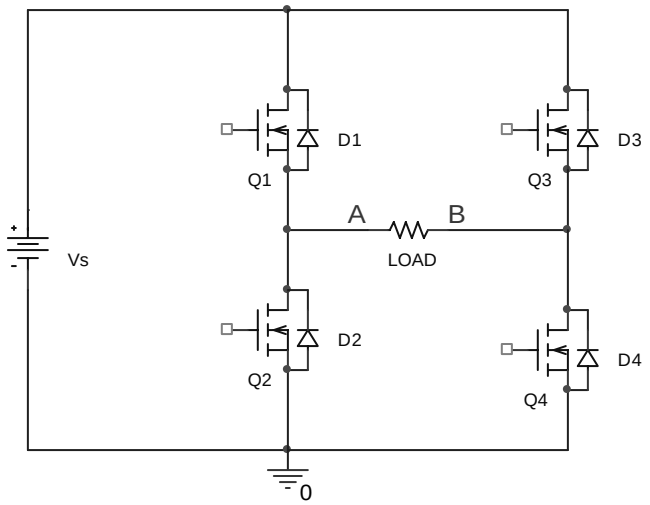


Fig. 5.2.3.3.7: Block representation of the voltage sensor circuit used

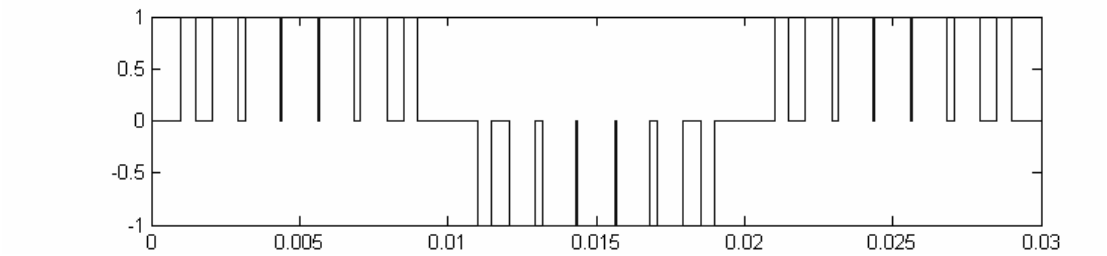
5.2.3.3.8 INVERTER SWITCH BRIDGE

The output of the inverter stage is fed to the filter and the output of the filter has to be connected to the grid. So, the inverter has to protect the back flow of the power from grid to the inverter.

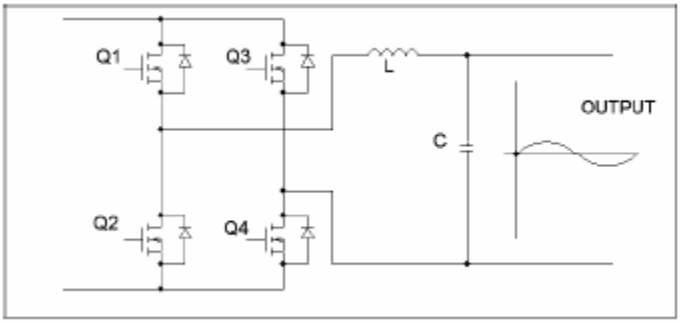
Such protection of the inverter was ensured by choosing the three level PWM scheme. Let us consider a single-phase full bridge inverter as shown in Fig. 5.2.3.3.8 (a).



(a)



(b)



(c)

Fig. 5.2.3.3.8: (a) Single-phase full bridge inverter. (b) Voltage wave shape across resistive load. (c) Inverter with the filter as a load.

The inverter has four switches Q_1, Q_2, Q_3, and Q_4. As the switches Q_1 and Q_4 are turned ON, voltage $+V_s$ is impressed across the load ($V_{AB} = +V_s$). When the switches Q_1 and Q_4 are turned OFF and the switches Q_2 and Q_3 are turned ON, a voltage of $-V_s$ is impressed across the load ($V_{AB} = -V_s$). The output of the inverter is shown in Fig. 5.2.3.3.8 (b). The switches Q_1, Q_2, Q_3, and Q_4 are switched by a PWM pattern so that the output voltage contains fewer harmonic.

Now, let us consider the case when a LC filter is connected as the load of the bridge as shown in Fig. 5.2.3.3.8 (c). As the switches Q_1 and Q_4 are turned ON, voltage $+V_s$ is impressed across the load ($V_{AB} = +V_s$). When the switches Q_1 and Q_4 are turned OFF and the switches Q_2 and Q_3 are turned ON, a voltage of $-V_s$ is impressed across the load ($V_{AB} = -V_s$). Since value of Vs is not less than 400V there is no chance of back flow of power. The diodes D1, D2, D3 and D4 provide free wheeling path.

As the switches of the PWM inverter are alternately turned ON in pairs, i.e. Q1, Q4 are ON during positive half-cycle of the Grid voltage and Q2, Q3 are ON in the negative half cycle, hence there is no chance of power flow into the system from grid.

5.2.3.3.9 DESIGN OF SWITCHES

The bridge network contains four switches. The targeted efficiency of the switching stage of the inverter is ***99***%.

Maximum input voltage to the bridge, $\boldsymbol{V_{in\text{-}max} = 800V}$
Minimum input voltage to the bridge, $\boldsymbol{V_{in\text{-}min} = 400V}$
Maximum output power of the inverter, $\boldsymbol{P_{out}: 1kW}$
Maximum switching current $\boldsymbol{I_{d\text{-}max} = 1kW/400 = 2.5A}$
Targeted efficiency $\boldsymbol{\eta = 99\%}$
Maximum average switching loss (per switch) $\boldsymbol{P_{sw\text{-}loss} = 5W}$
Maximum ON resistance, $\boldsymbol{r_{ds(on)} = P_{sw\text{-}loss} / I^2_{d\text{-}max} = 800m\Omega}$

For safety of operation and cost-efficiency trade off the MOSFETs of ***900V 10A 1Ω*** were selected. We chose **FQA11N90C** from FAIRCHILD Semiconductor.

5.2.4 OUTPUT FILTER DESIGN

The transfer function of LC filter (to be connected at the output of PWM inverter) is determined considering non-ideal capacitor and inductor. As our carrier frequency varied from 3.2 kHz (for generating 50 Hz output) to 3.84 kHz (for generating 50 Hz output), we used a filter having a cut-off frequency of around 1 kHz. ***L= 5 mH*** and ***C= 5 μF*** were chosen for this purpose. This results in about 3^o phase shift at 50/60 Hz. Such phase shift was balanced by shifting the PWM patterns properly. The resistance of the inductor is kept below 0.02 for obtaining minimal phase shift at 50/60 Hz.

6 SIMULATION RESULTS

The performance of the PWM scheme is simulated to see the capability of the PWM controller for generating efficient PWM patterns that provide fewer harmonics in output voltage. The simulated output for 14 carrier pulses is shown in Fig. 6(a). The FFT of the simulated result using 64 carrier pulses (used in our scheme) is presented in Fig. 6(b), which indicates that a filter of 1 KHz cut-off is sufficient for obtaining a low distortion output.

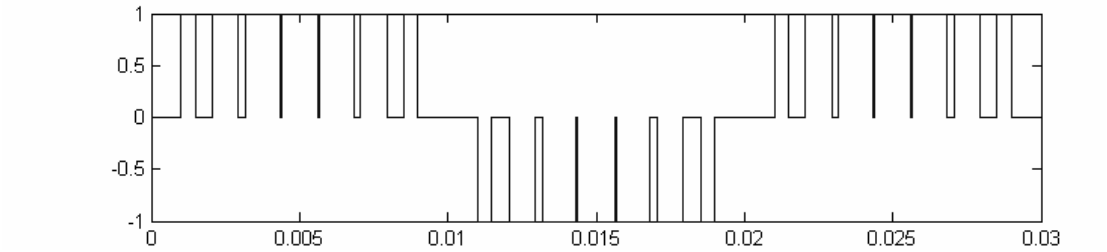


Fig. 6: Simulation results. (a) PWM pulses for 14 pulse per period.

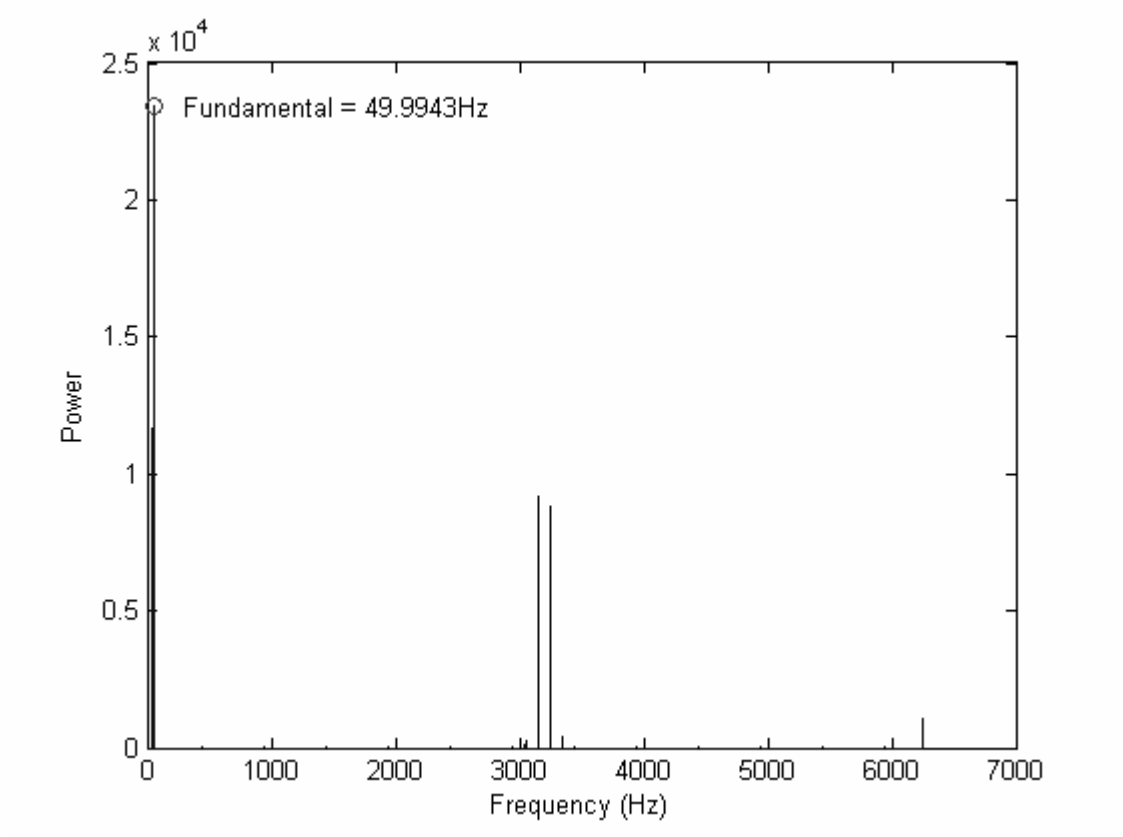


Fig. 6: Simulation results. (b) FFT of 64 pulses PWM (used in this project).

7 EXPERIMENTAL RESULTS

In this section, we are presenting some photographs of output waveforms taken at two different conditions, and the FFT of the same waveforms (Fig. 7.1 & 7.2), which validated our prediction of a low DF output. Efficiency of our system was also measured for different output condition in standalone mode and tabulated in this section. And, our scheme responds pretty well in normal and abnormal grid conditions. The photograph of BUET Utility Interactive Inverter System is also given in this section (Fig. 7.3).

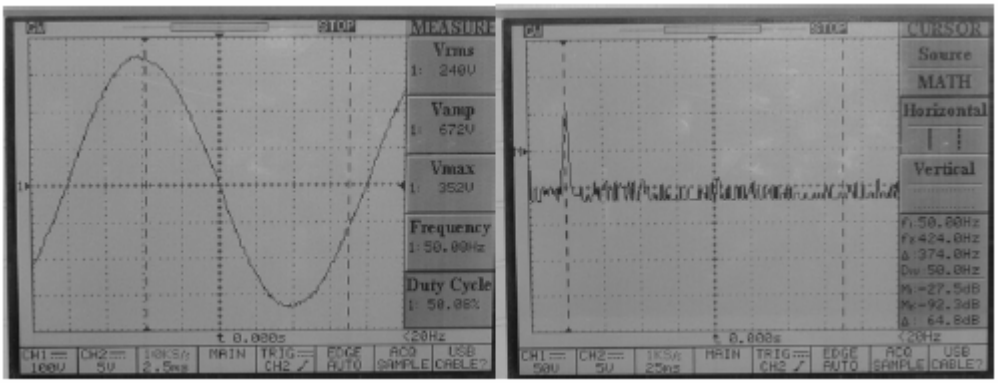


Fig. 7.1: Photograph of output waveform indicating a 240V, 50 Hz AC. The load at the present condition is 750W and the system is operating in Grid mode. The FFT of the same waveform is presented at right hand side indicating low distortion.

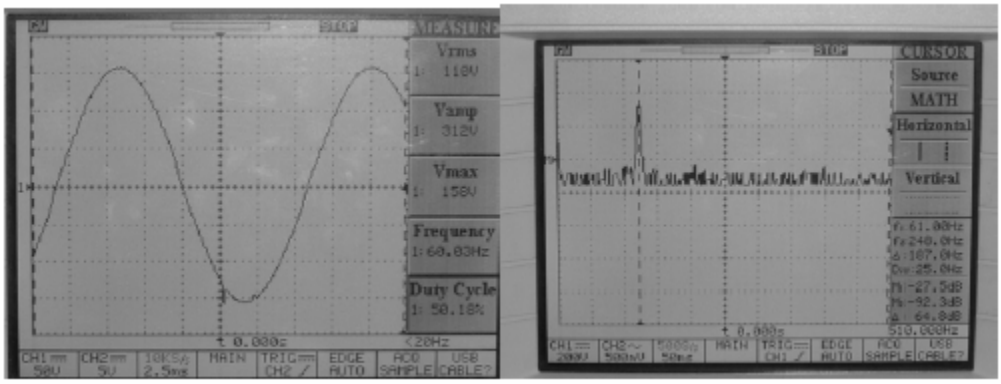


Fig. 7.2: Photograph of output waveform indicating a 110V, 60 Hz AC. The load at the present condition is 850W and the system is operating in Standalone mode. The FFT is presented in the RHS.

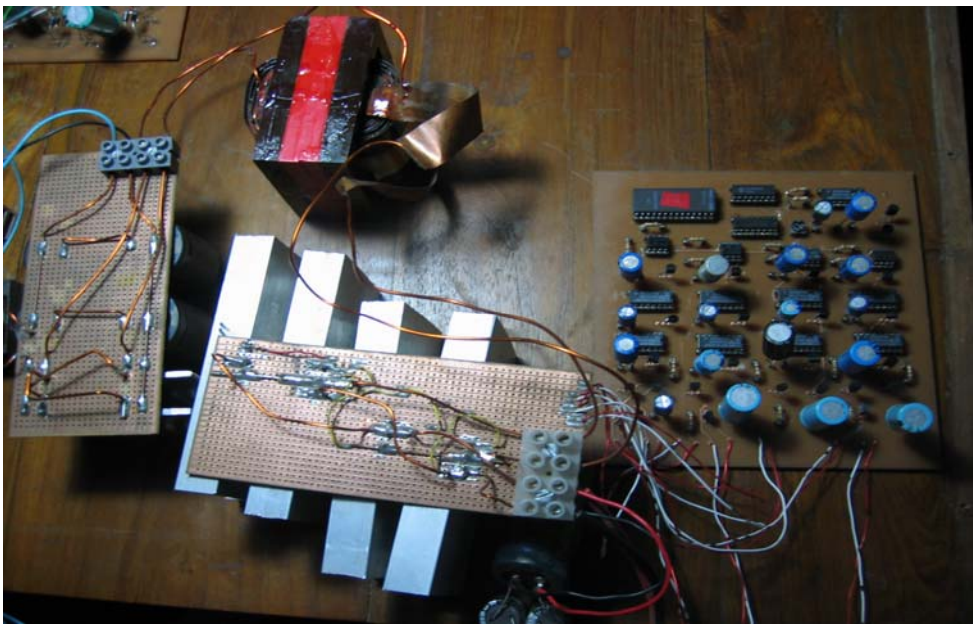


Fig. 7.3: Photograph of PCB boards. (a) DC-DC converter module board.

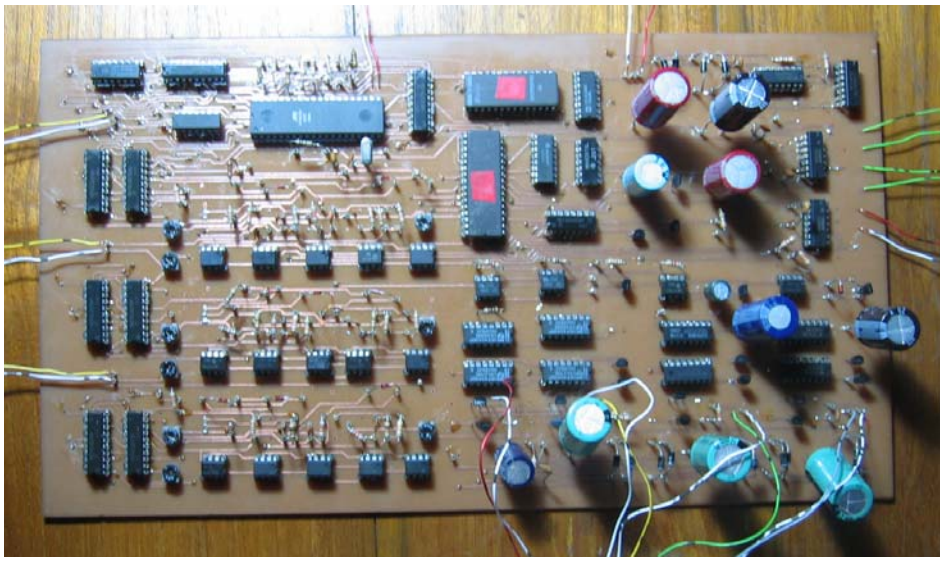


Fig. 7.3: Photograph of PCB boards. (b) Microcontroller Module Board.

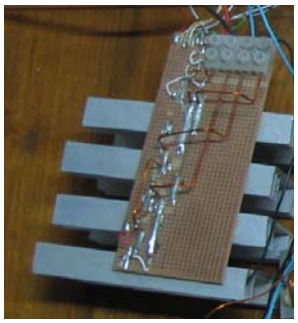


Fig. 7.3: Photograph of PCB boards. (c) PWM Inverter switching module.

7.1 OBTAINED DATA

The scheme is tested using a 30~60V DC supply, capable of providing a maximum output power of 1kW. Efficiency is measured in Standalone mode both for 110V (60Hz) and 240V (50Hz) output conditions. The current, voltage and power are measured by a clip-on type digital power meter (KYORITSU 2011). Results of the experimental performance are shown in Table 7.1.1, 7.1.2 & 7.1.3.

Table 7.1.1: Experimental results (110V/60Hz).

Input Current (A)	Input Voltage (V)	Input Power (W)	Output Voltage (V)	Output Power (W)	%Efficiency
2.75	30	82.5	111	72.50	87.9
5.25	30	157.5	111	137.20	87.1
8.00	30	240.0	111	208.50	86.8
12.00	30	360.0	111	308.35	85.6
15.00	30	450.0	110	383.10	85.1
20.00	30	600.0	111	500.20	83.4
25.00	30	750.0	110	629.20	83.9
30.00	30	900.0	111	760.50	84.5
34.00	30	1020.0	111	850.80	83.4

Table 7.1.2: Experimental results (240V/50Hz).

Input Current (A)	Input Voltage (V)	Input Power (W)	Output Voltage (V)	Output Power (W)	%Efficiency
8.0	35	280.00	240	250.1	89.3
12.0	35	420.00	240	368.3	87.7
16.5	35	577.50	239	502.2	86.9
18.0	40	720.00	240	620.0	86.1
18.5	45	832.50	241	705.5	84.7
19.5	50	975.00	240	820.7	84.2
20.25	55	1113.75	240	933.0	83.7

Table 7.1.3: Abnormal Condition detection in Grid Mode, along with the Grid and Output Voltage.

110V (60Hz)		240V (50Hz)	
Grid Voltage (V)	Output Voltage (V)	Grid Voltage (V)	Output Voltage (V)
80 (abnormal grid)	110 (Isolated)	170 (abnormal grid)	240 (Isolated)
86 (abnormal grid)	110 (Isolated)	180 (abnormal grid)	240 (Isolated)
90	90	190 (abnormal grid)	240 (Isolated)
95	95	200	200

100	100	210	210
105	105	220	220
110	110	240	240
115	115	250	250
120	120	260	260
125	125	270	270
130 (abnormal grid)	110 (Isolated)	280 (abnormal grid)	240 (Isolated)
135 (abnormal grid)	110 (Isolated)	300 (abnormal grid)	240 (Isolated)

Hence, the results show that the efficiency of the system is above 83% in all load conditions. The losses may have incurred in the switches and in the cores of the transformer. We are working on determining the exact reason, and expecting to reach an efficiency of above 90%. Table 3 indicates that our system can detect the abnormal voltage conditions pretty well and the output voltage closely follows the grid voltage.

8 PERFORMANCE EVALUATION

The Efficiency vs. %Load is shown in Fig 8.1. A rough cost analysis is presented in Table 8.1, considering the components used in the high power sections only, using the excel sheet provided in [4]. Finally, a cost evaluation is done based on the component used and the excel sheet, provided online by the IFEC organizers. The performance analysis is given in Table 8.2 from which it is obvious that almost all the requirements of IFEC are fulfilled. The only short coming is in the efficiency. The required efficiency was 90% whereas BUET Inverter's efficiency is 83%.

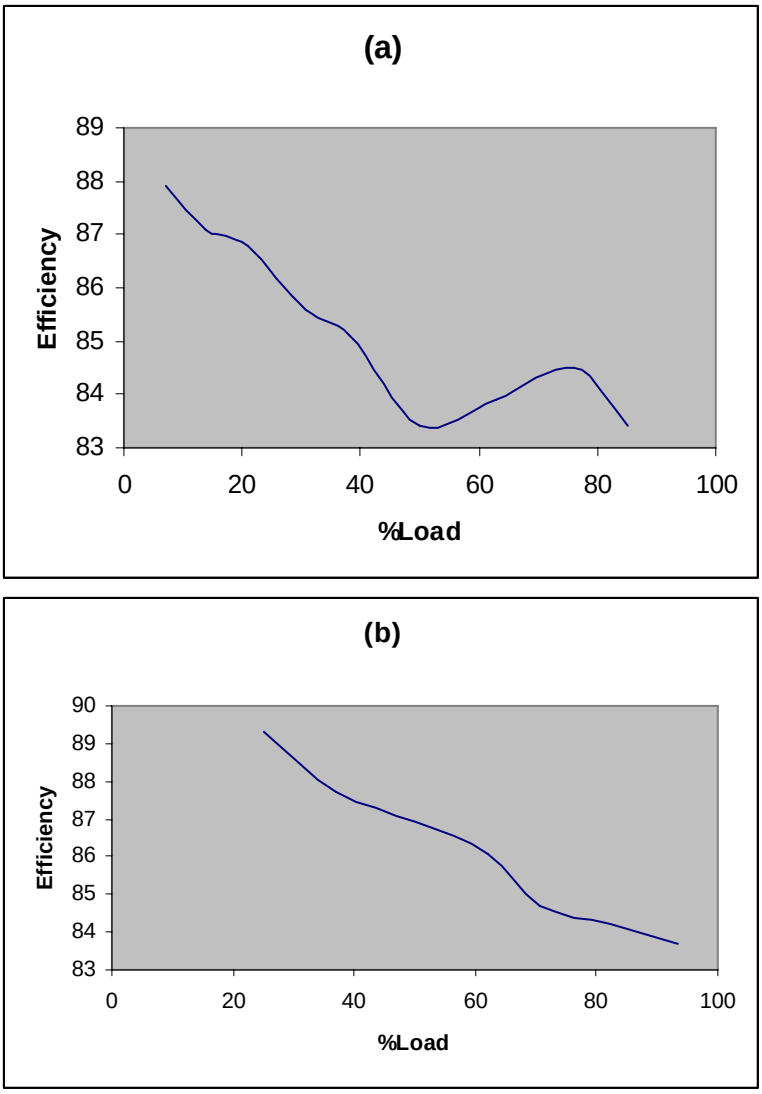


Fig. 8.1: Efficiency vs. %Load. (a) 110V/60Hz. (b) 240V/50Hz.

Table 8.1: Cost Analysis.

DEVICE	QTY	DESIG	UNIT	MEASURE	VOLT (Vpk)	VOLT (Vrms)	CUR (Avg)	CUR (Arms)	POINTS PER UNIT	POINTS
DIODE	4	D1,2,3,4			1000		5		1.26	5.03
MOSFET	4	Q1,2,3,4			100		40		2.98	11.91
MOSFET	4	Q5,6,7,8			900		5		3.11	12.45
CAP (ALUM)	1	C1	6800	uF	85				3.45	3.45
CAP (ALUM)	1	C2	400	uF	400				4.48	4.48
CAP (FILM)	1	C3	5	uF	400				2.15	2.15
POWER RESISTOR	4	R1	5	W					0.60	2.40
CHOKE	1	L1	100	UH				40	7.56	7.56
CHOKE	1	L2	2	UH				5	2.47	2.47
CHOKE	1	L3	5000	UH				10	18.38	18.38
TRANSFORMER	1	T1				60		40	4.45	4.45
LOSSES			165	W					6.88	6.88
CONTROL	4 Boards: Two for DC-DC Converter, one for PWM Inverter, one for Microcontroller Board									16.32
PACKAGING										12.24
OTHER (EXPLAIN)										
TOTAL										110.17

Table 8.2: The performance evaluation of the prototype designed by BUET team.

Design Item	***FEC Requirement***	***BUET team performance***
Manufacturing cost	Less than US$200/kW when scaled to high-volume production (approximately 100,000 units/year)	Less than US$120 per kW
Complete package weight	Mass less than 3 kg	Mass less than 2.5 kg
Output power capability	The ranges that will be tested are 110 V +15% -20%, at 60 Hz ± 2% and 240 V +15% -20%, at 50 Hz ± 2%. The unit must disconnect automatically from the utility grid and keep a stand-alone emergency load (maximum 250 W) if an external blackout or abnormal operating conditions occur with the grid interconnection. The unit will also be tested in stand-alone for powering a 1 kW resistive load. The voltage tolerance should be ±10% for all power range.	Tested in the range 110 V +15% -20%, at 60 Hz ± 2% and 240 V +15% -20%, at 50 Hz ± 2%. The unit disconnects itself from the utility grid and keeps a stand-alone emergency load (maximum 250 W) if an external blackout or abnormal operating conditions occur with the grid interconnection. It can response to the grid conditions within 2 to 10 grid cycles.
Stand-by (tare) losses, i.e., when the inverter is on, but not producing power (low load).	Less than 3% of full rating.	Less than 1% of 1kW
Harmonic quality	In accordance to IEEE 519 and IEEE 1547.	Within the requirement
Load	The inverter will be tested in grid-connected mode and will have to be able to provide all the output power range at unity power factor. The inverter has to	The inverter capable of automatically detecting blackout, disconnecting from the grid and keeping an auxiliary load of up to 250 W operating normally. The

	automatically detect blackout, disconnect from the grid and keep an auxiliary load of up to 250 W operating normally. The inverter will also be tested in stand-alone. In stand-alone, it has to generate either 50 Hz or 60 Hz (maybe configured by jumpers) and capable to power a resistive load of 1000 W	inverter was also tested in stand-alone. In stand-alone, it is capable of generating either 50 Hz or 60 Hz (configured by switch) and capable to power a resistive load of 1000 W.
Overall energy efficiency	Higher than 90% for a 1.0 kW resistive load. Additional scoring points will be awarded for efficiencies higher than 90%.	Higher than 83%.
Protection	Over current, over voltage, short circuit, over temperature, under voltage. No damage caused by output short circuit. The inverter will be surely tested against short circuit. The inverter must shut down if the input voltage dips below the minimum input. IEEE Std. 929 is a useful reference.	Can detect and protect itself from over current, over voltage, short circuit, under voltage within 2 to 10 fundamental cycles.
Acoustic noise	No louder than conventional domestic refrigerator. Less than 50 dBA sound level measured 1.5 m from the unit.	No louder than conventional domestic refrigerator.
Galvanic isolation	Galvanic isolation must be provided as a safety requirement. A grounding connection must be available.	Galvanic isolation is provided.

9 PROSPECT OF THIS PROJECT IN BANGLADESH

Now-a-days developing countries in the world are facing some major problems in their energy sector. Many developing countries do not have much natural (oil, gas) energy sources. As a result they are not able to fulfill their energy requirements. Even developed countries are facing problems in finding new mines or establishing new power plants. Existing power sources are not environment friendly. So a lot of individuals are now looking for other energy sources like sunlight. Solar cells can generate energy from sunlight but the efficiency of its hardware is very poor. So research like this IFEC project will surely help in developing new hardware prototypes to increase the efficiency up to a minimum margin and reduce the cost.

Bangladesh is also facing problems with her energy sources although she has huge amount of resources. But there is lack of utilization, especially in many rural areas where we do not have any power cables reached yet. But we have a huge amount of sunlight in all the places in our country throughout the year. So solar cells can be a good solution for this. If a device can be made which can generate energy as well as store it and thus cost is minimized, the people in those areas can create their own power systems at home. So our work can be beneficial to develop technologies in these fields.

10 FUTURE PLANS

In this scheme there is a scope of development in many areas. These modifications can uphold the project work more efficiently and more precisely. Some are listed below:

a. The overall efficiency of the inverter system is above 83%. BUET team designed the power components properly but due to market limitations could not select proper devices from market. The efficiency may be improved by choosing designed devices.
b. This project can be used in large scales of energies by increasing the transformer size and making necessary changes in the control circuitry.
c. By taking necessary steps, safety measure of this circuit can be increased so that no reverse current can flow. It ensures virtually zero probability for accident of machine.

11 CONCLUSION

After a long hard work, BUET team has finally completed the project that really works well fulfilling almost all the requirements stated. The performance of the system is tested for different output conditions, indicating moderate level of efficiency. The synchronization with the grid is inherent in our system, which is mandatory when power is to be fed to a grid from an energy source. The scheme adopts a novel strategy for high-resolution PWM pattern generation without using a high speed DSP, which helps generating a low distortion output. A complete lifetime study and different safety measures are tested. It appears that our project is a successful one.

12 REFERENCE

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