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# Gate C-V Characteristics of Si MOSFETs with Uniaxial Strain Along <110> Direction

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**Abstract – Gate C-V characteristics of nMOSFETs fabricated on 100 silicon and subjected to a uniaxial strain applied along the <110> direction are studied. MOS electrostatics is calculated by solving self-consistent Schrödinger-Poisson equations including wave-function penetration into the gate dielectrics. It is observed that the gate capacitance increases in strong inversion with strain, but is relatively unaffected by strain in depletion region. This is due to the changes in the electron quantization mass and density of states effective mass with strain. We have also found that the effect of strain on the gate capacitance is not sensitive to changes in the substrate doping density.**

## I. Introduction

MOS devices have entered the nanometer regime in the past decade [1]. 65 nm node has been commercially reached in 2007. Further scaling of MOS devices is facing several technological challenges. Nonconventional substrates are recently introduced to increase device speed and reliability. Biaxially strained Si MOSFETs have been widely studied for enhanced mobility of charge carriers [2, 3]. Uniaxially strained Si MOSFETs [4] have become more popular in recent days. Uniaxial strain also enhances carrier mobility [5]. The uniaxial straining process is simpler and more compatible with the conventional CMOS technology. By uniaxial strain different types of strain can be applied for pMOS and nMOS devices in a cMOS circuit. Mobility enhancement due to uniaxial strain has extensively been studied [6, 7], but gate C-V characteristics of uniaxially strained MOSFETs have received less attention even though the C-V characteristics is an important tool for characterizing MOS devices.

In this work a self-consistent quantum mechanical simulator is developed to model gate C-V characteristics of nMOS devices with uniaxially strained silicon channel. Uniaxial tensile stress is applied in the <110> direction. <110> direction is taken for its wide practical use in 100 silicon as the transport direction. Tensile stress is commonly applied to nMOSFETs for mobility enhancement. Proper band splitting and effective mass change due to strain are considered. The model is used to study how uniaxial tensile strain affects the gate C-V characteristics of nMOS devices. Physical insights into the effects of strain are also discussed.

## II. Theory

### A. Band splitting due to uniaxial strain

For relaxed 100 silicon, two separate valleys of conduction bands ($\Delta_2$ and $\Delta_4$) are at a degenerate state. Uniaxial stress removes this degeneracy and there is a splitting between the two valleys. Uniaxial stress also introduces a hydrostatic shift of the mean position of the conduction band. Similarly heavy hole and light hole bands also become nondegenerate under uniaxial stress. Fig. 1 shows the evolution of the energy bands under a uniaxial tensile strain.

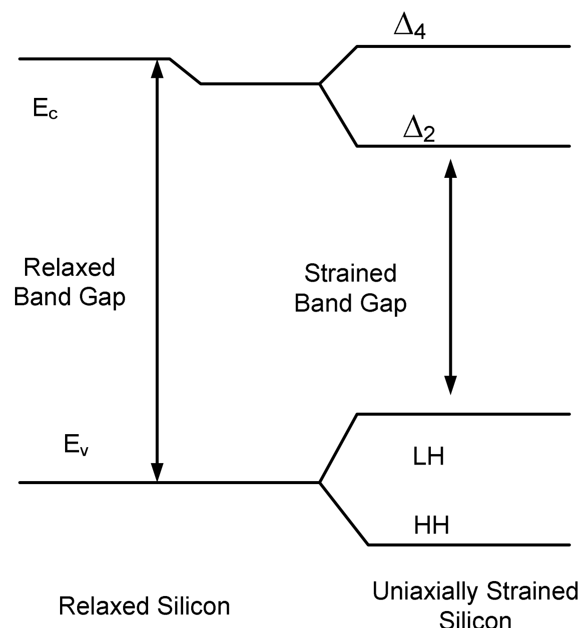


**Fig. 1 Band splitting of relaxed 100 silicon under uniaxial tensile stress. $\Delta_2$ and $\Delta_4$ are the two conduction band valleys, LH and HH are for light hole and heavy hole, respectively.**

Expressions for splitting of conduction band under a tensile stress along the <110> direction are described in [8] as,



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$$\Delta E_c^i - \Delta E_c^0 = -\frac{1}{3}(S_{11} - S_{12})\Xi_u X \text{, for } \Delta_2 \text{ band,}$$

$$\Delta E_c^i - \Delta E_c^0 = \frac{1}{6}(S_{11} - S_{12})\Xi_u X \text{, for } \Delta_4 \text{ band,}$$

$$\Delta E_c^0 = \Delta E_{g0} - |E_{\varepsilon\varepsilon}| - \frac{1}{3}(S_{11} - S_{12})\Xi_u X \text{,and}$$

$$\Delta E_{g0} = (\Xi_d + \frac{1}{3}\Xi_u - a)(S_{11} + 2S_{12})X \cdot$$

Here,
$\Delta E_c^0$ ≡ Hydrostatic band shifting of the conduction band,
$\Delta E_c^i$ ≡ Band splitting for the *i*th valley,
$\Delta E_{g0}$ ≡ Change in the energy band gap,
$X$ ≡ Applied stress,
$S_{11} = 8.63\times10^{-12}$ N$^{-1}$m$^2$,
$S_{12} = -2.13\times10^{-12}$ N$^{-1}$m$^2$,
$\Xi u = 8.6$ eV, and
$\Xi_d + \frac{1}{3}\Xi_u - a = 3.8$ eV.
$2|E_{\varepsilon\varepsilon}|$, the splitting between light hole and heavy hole bands at the band edge, is given by

$$|E_{\varepsilon\varepsilon}| = \frac{1}{2}\left[b^2(S_{11} - S_{12})^2 + 3\left(\frac{d}{2\sqrt{3}}S_{44}\right)^2\right]^{1/2} |X|$$

Here,
$b = 2.4$ eV,
$d = 5.3$ eV,
$S_{44} = 12.49\times10^{-12}$ N$^{-1}$m$^2$.

## B. Effective mass variation

Uniaxial strain causes the curvatures of the energy band structures to change. As effective masses depend on the curvature of energy bands, uniaxial stress changes effective masses. We follow the expressions given in [9] to model the variation of effective masses with uniaxial strain applied along <110> direction.

$$m_x = 0.918 + 0.0236X^2$$
$$m_y = 0.196 - 0.016X$$
$$m_z = 0.196 + 0.029X$$
$$m_{di1} = \sqrt{m_y m_z}$$
$$m_{z1} = m_x$$
$$m_{di2} = \sqrt{m_x m_y}$$
$$m_{z2} = m_z$$

Here, $X$ is the applied stress in GPa. Subscript 1 stands for $\Delta_2$ valley and subscript 2 stands for $\Delta_4$ valley.

## C. Self-consistent solver

A self-consistent Schrödinger-Poisson solver is developed to simulate gate C-V characteristics [10]. In the first part, Schrödinger's equation is solved using the logarithmic derivative technique of the retarded Green's function [11]. Open boundary condition is used at the silicon-gate-oxide interface to include penetration of wave functions into the gate dielectric. Our open boundary condition, that considers zero electric field deep inside the gate electrode, as well as deep inside the bulk silicon, incorporates wave function penetration effect naturally without introducing any unphysical artifact. In the second part, Poisson's equation is solved for the combined silicon-oxide regions to include the charge in gate-oxide region due to wave function penetration. Finite difference method is applied and non-uniform grid spacing is used to improve computational efficiency.

# III. Results

Fig. 2 shows the gate C-V characteristics of nMOSFETs with relaxed and uniaxially strained silicon channels. Three different stress levels along the <110> direction are considered. Here gate oxide thickness $T_{ox}$ = 2 nm, doping density $N_a = 10^{18}$ cm$^{-3}$. Flatband voltage is assumed to be zero in all calculations.

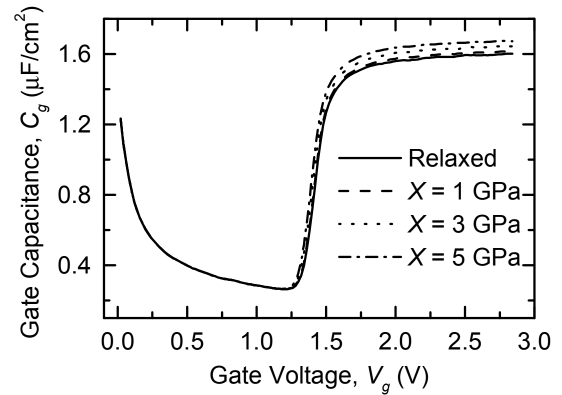


**Fig. 2 Gate C-V characteristics of relaxed and uniaxially strained Si MOSFETs.**

It is observed that uniaxial strain along the <110> direction has no effect on the gate capacitance in the depletion region and has a small effect in the weak inversion region. There is no shift in the flatband voltage due to uniaxial strain. However the gate capacitance in strong inversion increases under strain. Gate capacitance in strong inversion is increased by 2.7 % when 3 GPa stress is applied. It is also observed that uniaxial strain has a small effect on the threshold voltage $V_T$. This is in agreement with [12] where it is shown that compared to the biaxially strained MOSFETs, the threshold voltage shift is much smaller in uniaxially strained MOSFETs.

To investigate the factors influencing changes in gate capacitance under strain, we calculate the depletion width, band bending due to depletion charges and the total semiconductor charges as functions of the gate voltage for relaxed and strained silicon channel in Figs. 3, 4 and 5, respectively. We find that uniaxial strain has no effect on the depletion properties. The depletion width, consequently the depletion band bending and the depletion charge remain unaffected by strain. The increase in the total charge due to strain in strong inversion, as observed in Fig. 5, is due to increased charge in the inversion region.

Inversion capacitance ($dQ_{inv}/d\varphi_s$) as a function of gate voltage is shown in Fig. 6. It is clearly seen that $C_{inv}$ increases with increase in uniaxial stress for a given gate



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voltage in strong inversion. Strain affects the inversion charges in two ways. First, strain modifies the bandgap $E_g$ and second, strain changes the effective masses of electrons. For MOSFETs fabricated on 100 silicon surface, uniaxial strain increases the quantization effective mass. Consequently the energies of the quasi-bound states are lowered relative to the conduction band minima. For a given gate voltage, the density of the inversion charges is increased, leading to an increase in $C_{inv}$.

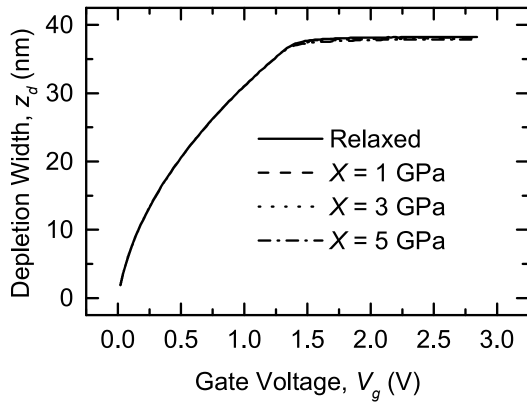


**Fig. 3 Depletion width as a function of $V_g$ for relaxed and strained Si MOSFETs.**

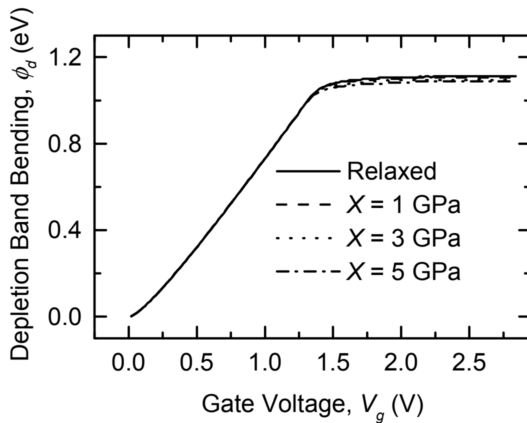


**Fig. 4 Band bending due to depletion charges for relaxed and strained Si MOSFETs.**

In Fig. 7 we show the C-V characteristics of strained MOSFETs calculated with (i) considering only the bandgap correction (ii) considering both the bandgap and the effective mass corrections. When modification of effective mass is neglected, strain has negligible effect on the gate C-V characteristics. The result shows that for the stress level considered in this work, the increase in the gate capacitance with uniaxial strain is primarily due to the increase in quantization and density of states effective masses and the bandgap modification does not play an important role.

Effect of doping density on C-V characteristics of strained Si devices is shown in Fig. 8. Here doping density level is $5\times10^{17}$ cm$^{-3}$. Gate capacitance in strong inversion is increased by 2.6 % for 3 GPa stress. This change is nearly the same as that observed in Fig. 2 for $N_a$ = $10^{18}$ cm$^{-3}$. Figs 2 and 8 suggest that the effect of

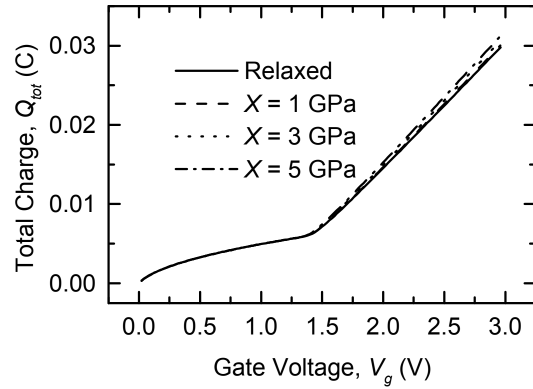


**Fig. 5 Semiconductor total charge versus $V_g$ for relaxed and strained Si MOSFETs.**

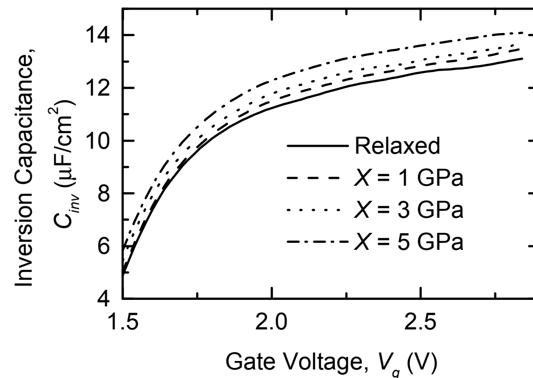


**Fig. 6 Inversion capacitance for relaxed and strained Si MOSFETs.**

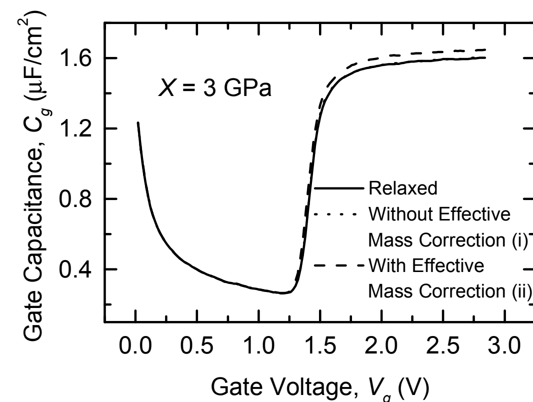


**Fig. 7 C-V characteristics with and without considering effective mass modification by strain.**



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uniaxial strain on the gate C-V characteristics is not very sensitive to changes in the substrate doping density.

## IV. Conclusion

We have developed a self-consistent quantum mechanical simulator to investigate the effects of uniaxial strain along the <110> direction on the gate C-V characteristics of MOSFETs fabricated on 100 silicon surface. Changes in both the bandgap and the electron effective masses are included in the model. We show that strain increases the inversion capacitance due to change in quantization and density of states effective masses. However for the stress levels considered in the work, depletion properties are unaffected by strain. It is also found that the effect of strain does not depend on the substrate doping density.

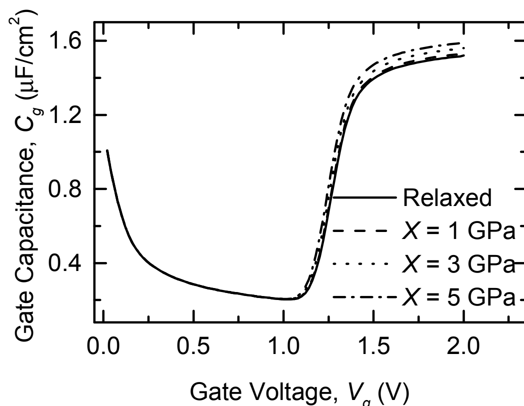


**Fig. 8 Gate C-V characteristics of strained and relaxed Si nMOSFETs for substrate doping density $N_a = 5\times10^{17}$ cm$^{-3}$.**

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