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AN IMPROVED PHYSICALLY BASED COMPACT C-V MODEL FOR MOS DEVICES WITH HIGH-K GATE DIELECTRICS

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ABSTRACT

An improved compact gate C-V model for MOS devices with high-*k* gate dielectrics is proposed. The model accurately includes the effect of wave function penetration into the gate dielectric. It is based on making λ, the exponent of the Airy function solution of the eigenenergy, dependent on the characteristics of the dielectric material and on the substrate doping density. Comparison with experimental C-V data shows that the proposed model is more accurate than existing model which consider a constant value of λ for all dielectric materials and doping densities.

1. INTRODUCTION

Aggressive scaling down of MOSFETs has continued to reduce the feature sizes into nanometer regime. The characteristics of such small devices are determined by quantum mechanical (QM) effects [1]. To overcome the serious technology difficulties related to using ultra-thin SiO_2 layers as the gate dielectric, alternative high-*k* materials are being considered as replacement of SiO_2. It has been shown recently that the gate C-V characteristics of high-*k* gate-dielectric MOSFETs are determined by the effects of wave function penetration into the dielectric material [2, 3].

In recent years, extensive amount of work has been done on QM effects on C-V characteristics [4, 5], and many numerical C-V simulators have been developed [6]. While these numerical simulators can provide accurate results, computationally efficient analytic C-V models are required for practical everyday device and circuit studies. Li et al. introduced a physically based compact C-V model for ultra-thin gate dielectrics considering the effects of wave function penetration [7]. In [7], the authors used a modified value for the exponent of the Airy function solution of the lowest quantized energy level. This value was determined from self-consistent numerical solution considering SiO_2 as the gate dielectric. Consequently, its use for simulating C-V with high-*k* gate dielectrics is questionable.

In this work, we have proposed a revised compact C-V model by considering the effect of dielectric material properties and substrate doping density on the exponent of the Airy function solution for holes of the eigenenergy. Results for electrons will be reported elsewhere.

2. THEORY

The triangular-potential approximation of the MOS potential well (the dielectric approximated as an infinite potential barrier and the slope of the potential in Si defined by the surface electric field) leads to Airy function solution for the eigenenergies as,

$$E_i \approx \left(\frac{\hbar^2}{2m^*}\right)^{\frac{1}{3}}\left[\frac{3}{2}\pi e F_s\left(i+\frac{3}{4}\right)\right]^{\frac{2}{3}} \qquad (1)$$

Where m^* is the quantization effective mass, i represents eigenstates with $i = 0$ corresponding to the ground state [1], and F_s represents the surface dielectric field. Although, Airy function solution provides compact analytic expression, it is inaccurate due to (i) linear approximation of the potential profile inside Si and (ii) the negligence of wave function penetration into the dielectric layer. Li et al. [7] proposed to overcome these limitations by changing the exponent of F_S from 2/3 by taking

wave function penetration and non-triangular potential profile into account. They suggested that the ground state subband energy of the holes could be written as,

$$E_1 - E_v \cong \gamma \left(\frac{|F_{ox}|cm}{MV} \right)^{\lambda} \qquad (2)$$

Here, E_v is the valance band edge at the Si-dielectric interface and F_{ox} is the effective oxide field at the Si-dielectric interface. λ is the modified exponent of the power law relationship. Li et al. calculated the compact C-V model parameters as, γ = 88 meV and λ = 0.64 for holes both in inversion (p-MOS) and in accumulation (n-MOS) [7]. This shows that even a very small deviation in the exponent (λ) from 2/3 is significant in C-V calculations. Since in [7] only SiO_2 is considered as the gate dielectric and effect of doping density of the substrate is neglected in the calculation of these parameters from numerical data, it is not expected that these values of γ and λ would be reliable for high-k gate dielectric MOS devices.

To improve the model of [7] for high-k gate dielectrics, we suggested that λ is in fact a function of both the dielectric properties (k, m^*_{ox}, and barrier height, ϕ_b) and the substrate doping density. It may be mentioned that the compact model is not very sensitive to the variation of γ. In order to include these effects on λ, we perform numerical calculation of E_1 for MOS structures with different dielectric materials and different substrate doping densities. By fitting these data with Eq. (2), the dependence of λ on dielectric properties and doping density may be determined.

3. DETERMINATION OF λ

To calculate λ from Eq. (2) self-consistent simulations were performed [5]. Our numerical calculation shows that for a given equivalent oxide thickness (EOT), λ is not sensitive to change in k or m^*_{ox}, rather among dielectric properties, depends only on ϕ_b. A typical plot for E_1 versus F_{ox} is shown in Fig. 1 for Y-O-Si (ϕ_b = 4.5 eV) gate dielectric material. Two different doping densities are used. A best fit line is also shown with value of λ specified.

To investigate in detail the dependence of λ on ϕ_b and substrate doping density (N_d for p-MOS and N_a for n-MOS) variation of λ with ϕ_b for different doping densities is shown in Fig. 2(a). In Fig. 2(b) variation of λ with doping densities for different ϕ_b is shown. In these cases, simulations were performed with Al as gate metal, k = 10 and EOT = 1 nm. From

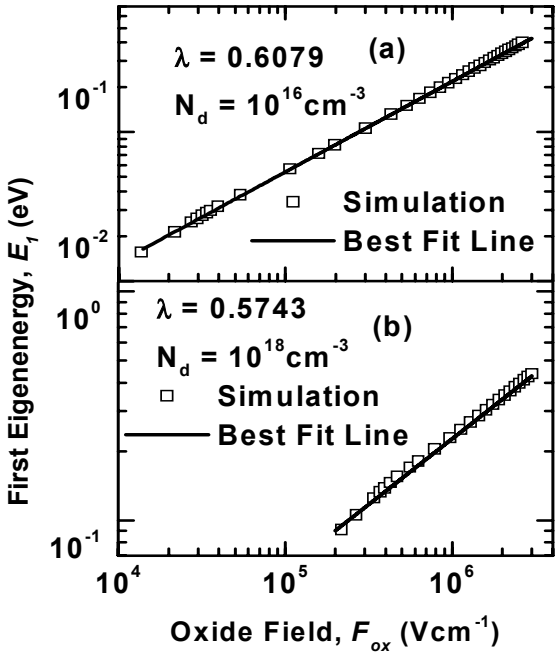

Fig. 1. E_1 vs. F_{ox} for Y-O-Si for two different doping densities with EOT = 1 nm. λ is determined from the slope of the corresponding best fit line.

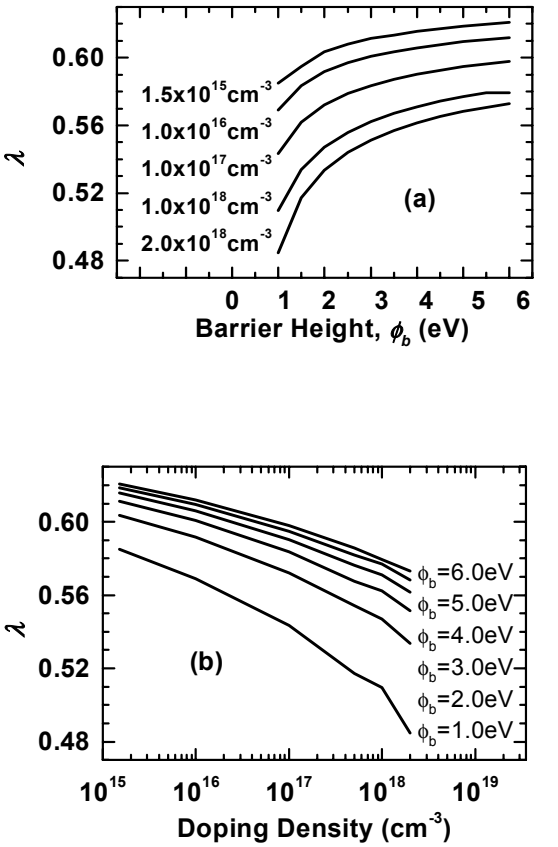

Fig. 2. (a) Variation of λ with ϕ_b for different doping densities. (b) Variation of λ with doping densities for different ϕ_b.

these plots we can estimate value of λ for any dielectric material and any substrate doping density. Use of this λ value in the compact model of [7] instead of 0.64 provides more accurate simulation of C-V calculation.

4. VERIFICATION OF THE MODEL

We verify our proposed model by comparing with two experimental C-V curves. Simulations are performed using λ value mentioned in [7] as well as those extracted from Fig. (2).

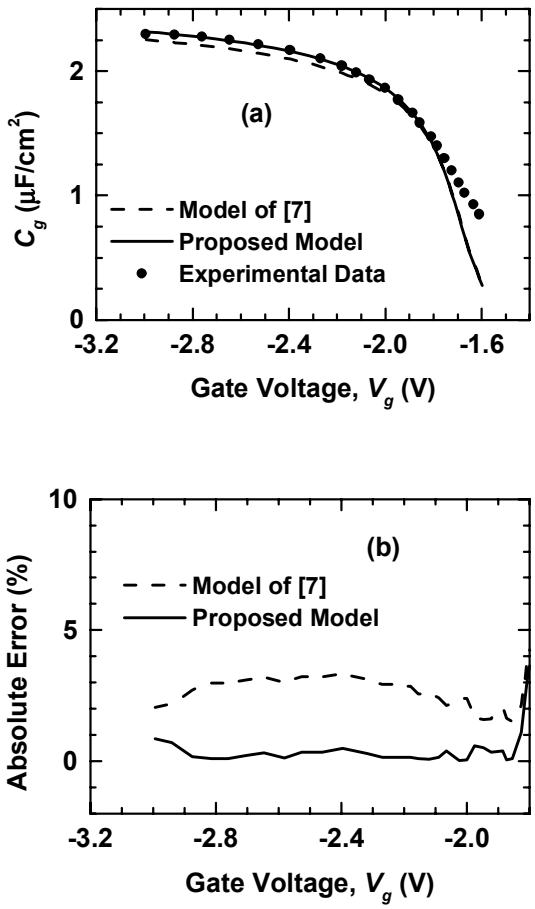

Fig. 3. (a) C-V curves for Y-O-Si as gate dielectric material. Here doping density $N_a = 10^{17}$cm^{-3}, EOT = 1.1nm. (b) Error curve for Y-O-Si as gate dielectric material.

Fig. 3(a) shows accumulation C-V curves for Y-O-Si dielectric. Experimental data is obtained from [8]. In our simulation we have used $N_a = 10^{17}$ cm^{-3}, EOT = 1.1 nm and $\phi_b = 4.5$ eV [3]. For these values of parameters, we extract from Fig. 2 that $\lambda = 0.595$. It may be mentioned that in the C-V simulation we have used the flatband voltage V_{FB} = -0.74 V from the experimental data. It is seen that under low bias voltage the two models are indistinguishable. But in strong accumulation, our proposed model is closer to experimental data. Fig. 3(b) shows that the relative error in strong accumulation is negligible when our proposed value of λ is used.

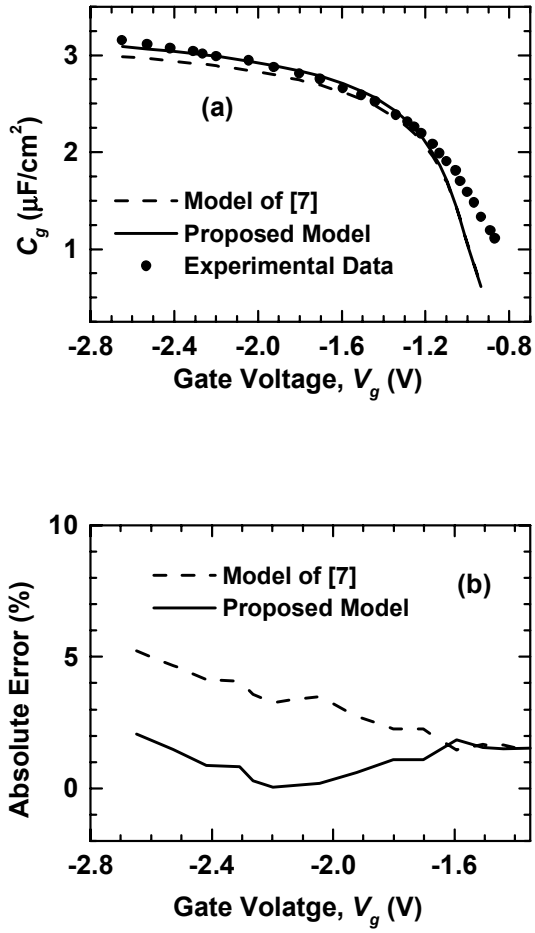

Fig. 4. (a) C-V curves for ZrO_2 as dielectric material. Here doping density $N_a = 2.1\text{x}10^{15}$ cm^{-3}, EOT = 0.88 nm. (b) Error curve for ZrO_2 as dielectric material.

Fig. 4(a) shows accumulation C-V for nitrided ZrO_2 gate dielectric. Experimental data is taken from [9]. The values of different parameters are $N_a = 2.1\text{x}10^{15}$ cm^{-3}, EOT = 0.88 nm and $\phi_b = 1.8$ eV. The value of λ as extracted from Fig. 2 is 0.60. Here V_{FB} = -0.80 V. It is again found that our proposed model simulates the C-V characteristics more accurately than the model of [7]. The model of [7] underestimates the slope of the C-V curve in strong accumulation, evidenced by the increasing error in Fig. 4(b). This is for the fact that ϕ_b for nitrided ZrO_2 is much lower than that of SiO_2 but this effect is absent in the model of Li et al.

5. CONCLUSION

We have proposed to improve the physically based, compact C-V model of [7] by incorporating the effect of dielectric-Si barrier height and doping density on the power law exponent of the relationship between the lowest eigenenergy and surface electric field. Comparison with experimental C-V data shows that incorporation of these effects is necessary for accurately simulating C-V characteristics of MOS structures with high-*k* gate dielectrics.

REFERENCES

[1] F. Stern, "Self-consistent results for n-Type Si inversion layers," Phys. Rev. B, vol. 5, pp. 4891-4899, 1972.

[2] M. M. A. Hakim and A. Haque, "Accurate modeling of gate capacitance in deep submicron MOSFETs with high-k gate-dielectrics," Solid State Electron., vol. 48, pp. 1095-1100, 2004.

[3] A. E. Islam and A. Haque, "Accumulation gate capacitance of MOS devices with ultra-thin high-k gate dielectrics: modeling and characterization," IEEE Trans. Electron Devices, vol. 53, pp. 1364-1372, 2006.

[4] S. Mudanai, L. F. Register, A. F. Tasch and S. K. Banerjee, "Understanding the effects of wave function penetration on the inversion layer capacitance of NMOSFETs," IEEE Electron Device Lett.,vol. 22, no. 3, pp. 145-147, 2001.

[5] A. Haque and M. Z. Kauser, "A comparison of wave-function Penetration effects on gate capacitance in deep submicron n- and p-MOSFETs," IEEE Trans. Electron Devices, vol. 49, no. 9, pp. 1580–1587, 2002..

[6] C. A. Richter, A. R. Hefner and E. M. Vogel, "A comparison of quantum-mechanical capacitance-voltage simulators," IEEE Electron Device Lett., vol. 22, no. 1, pp. 35-37, 2001.

[7] F. Li, S. Mudanai, L. F. Register and S. K. Banerjee, "A physically based compact gate C–V model for ultrathin (EOT ~ 1 nm and below) gate dielectric MOS devices," IEEE Trans. Electron Devices, vol. 52, no. 6, pp. 1148-1158, 2005.

[8] J. J. Chambers and G. N. Parsons, "Physical and electrical characterization of ultrathin yttrium silicate insulators on silicon," J. Appl. Phys., vol. 90, no. 2, pp. 918-933, 2001.

[9] R. Nieh, R. Choi, S. Gopalan, K. Onishi, C. S. Kang, H.-J. Cho, S. Krishnan, and J. C. Lee, "Evaluation of silicon surface nitridation effects on ultrathin ZrO_2 gate dielectrics," Appl. Phys. Lett., vol. 81, no. 9, pp. 1663-1665, 2002.