

Md. Itrat Bin Shams

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EDUCATION

MS in Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, August 2008. CGPA: 3.92 out of 4.00.

BS in Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology, November 2006. CGPA: 3.9447 out of 4.00, Rank: 3/135 (in EEE Department).

INTERNATIONAL ACHIEVEMENTS

Winner, IEEE Enterprize Award 2006.

Winner, Best Student Paper Award, International Conference on Electrical and Computer Engineering 2006.

Honorable Mention, IEEE International Future Energy Challenge competition 2005 (IFEC 2005).

Winner of award, Student Paper Contest 2007, IEEE ED Bangladesh Chapter, 3rd Position.

Travel and subsistence grant for EPEDC, ICTP (International Center for Theoretical Physics), Italy, 2008.

Travel and subsistence grant for Energy: Crisis and Future Outlook, National Research Center, Cairo, Egypt, 2010.

PUBLICATIONS

- 1 **M. Itrat B. Shams**, K. M. Masum Habib, Q. D. M. Khosru, A. N. M. Zainuddin and A. Haque, "On the physically based compact gate C-V model for ultrathin gate dielectric MOS devices using the modified Airy function approximation," **IEEE Transaction on Electron Devices**, Volume 54, Issue 9, Sept. 2007, Page(s): 2566 - 2569.
- ◇ **M. Itrat B. Shams**, Q. D. M. Khosru and A. Haque, "Effects of uniaxial strain on gate C-V characteristics of MOS devices," to be submitted in **Journal of Applied Physics**.
- ◇ **M. Itrat B. Shams** and A. Haque, "Threshold voltage variation in ultrathin MOS devices with uniaxially strained Si substrate," to be submitted in **IEEE Transaction on Electron Devices**.
- 2 **Md. Itrat Bin Shams**, K. M. Masum Habib, Rajib Mikail, Quazi Deen Mohd Khosru, A. N. M. Zainuddin and A. Haque, "An Improved Physically Based Compact C-V Model for MOS Devices with High-k Gate Dielectrics," International Conference on Electrical and Computer Engineering, ICECE 2006, Dhaka, Bangladesh. (**Best student paper award**)
- 3 **Md. Itrat Bin Shams**, "Signature Recognition by Segmentation and Regular Line Detection," IEEE Tencon 2007, Taiwan.
- 4 **Md. Itrat Bin Shams**, Md. Kawsar Alam and Quazi D. M. Khosru, "Effects of Uniaxial Strain on the Gate Capacitance of Double Gate MOSFETs," Proceedings of IEEE International Conference on Electron Devices and Solid-State Circuit 2008 (IEEE EDSSC), Hong Kong.
- 5 **Md. Itrat Bin Shams**, Quazi Deen Mohd Khosru and A. Haque, "Gate C-V Characteristics of Si MOSFETs with Uniaxial Strain Along $\langle 110 \rangle$ Direction," International Conference on Electrical and Computer Engineering, ICECE 2008, Dhaka, Bangladesh.

RESEARCH INTERESTS

Quantum mechanical simulation of nanoscale devices, solid-state physics study, III-V heterostructures, strained silicon devices.

RESEARCH WORKSHOPS ATTENDED

EPEDC, International Center for Theoretical Physics, Trieste, Italy, Mar. 17-21, '08.

EDSSC, IEEE International Conference on Electron Devices and Solid-State Circuit, Hong Kong, '08.

RESEARCH EXPERIENCES

Semiconductor Device Simulation Developed a compact model and expressed an exponent value to simulate C-V characteristic of MOS devices, as a function of barrier height of dielectric and doping density of bulk silicon.

Strained Silicon Structure Modeling of MOS devices with uniaxially strained silicon to study the electrostatic properties.

PROFESSIONAL EXPERIENCES

Faculty Member, Department of Electrical and Electronic Engineering, BUET (November '06 - Present)

Courses Taught: Electrical Properties of Materials, Electronic Devices and Circuits, Basic Electrical Circuits, Microprocessor and Interfacing Laboratory, Electrical Services Design, Numerical Techniques, Electrical Circuit Simulation Laboratory.

Developed laboratory manual for Microprocessor Laboratory and Electrical Services Design.

Prepared a lecture series for Electrical Services Design,

http://teacher.buet.ac.bd/itrat/Lecturer_eee_buet.html.

PROFESSIONAL AFFILIATIONS

The Institute of Electrical and Electronics Engineers (IEEE).

IEEE Electron Devices Society.

nanoHUB.org (registered user of nanoMOS, Schred).

ACADEMIC HONORS

Board Scholarships in every level.

Dean's list awards in all levels.

Merit scholarships in all semesters.

Outstanding student award from Titumir Hall.

LEADERSHIP EXPERIENCES

Student Activities Chair, IEEE Bangladesh Section, 2007

Organized IEEE Sparks quiz contest in 2007.

Organized IEEE Bangladesh Section Student Paper Contest 2006-2007.

Organizer of the new membership drive program, scientific seminars and talks.

Designer of the proceedings of the Student Paper Contest 2007, IEEE ED Bangladesh Chapter.

Executive committee member, IEEE ED Bangladesh Chapter, 2009

Co-organizer, IEEE ED Mini Colloquium, 2009.

Co-organizer, IEEE ED Bangladesh Chapter Student Paper Contest 2009.

Activities Chair (2005-Present), EEE Undergraduate Student Research Group, BUET.

Class Representative (2001-'06), EEE Department, Section A, Class of 2006.

REPRESENTATIVE IN THE INTERNATIONAL ARENA

Attended the workshop EPEDC 2008 organized by ICTP in Italy.

Attended Energy: Crisis and Future Outlook, National Research Center, Cairo, Egypt, 2010.

RELEVANT COURSEWORK

Undergraduate Courses Basic Electronics, Electrical Engineering Materials, Semiconductor Devices, VLSI Circuits.

Graduate Courses MOS Devices, Advanced VLSI Circuits, Compound Semiconductor Devices, Electric and Magnetic Properties of Materials, Applied EM Theory.

EXTRA-CURRICULAR ACTIVITIES

Guiding one undergraduate group to develop a compact model to simulate gate leakage current in MOS devices.

Helping several students to build up a self-consistent model of electronic devices.

Faculty advisor for Electrical Day, day long program arranged by the department.

One of the organizers in 60 years anniversary program of BUET.

Md. Itrat Bin Shams

Publications and International Achievements

Selected Publications

1. M. Itrat B. Shams et al. "On the physically based compact gate C-V model for ultrathin gate dielectric MOS devices using the modified Airy function approximation"

Journal: IEEE Transaction on Electron Devices

Volume: 54

Number: 9

Pages: 2566-2569

Abstract: The exponent of the modified Airy function solution of the quantized energy levels in the MOS potential well, used in the physically based, quantum-mechanical (QM) compact gate C-V model of Li has been found to be dependent on the barrier height at the Si-dielectric interface and the substrate doping density. An empirical equation is proposed for considering these effects. Comparison with experimental C-V data of MOS devices with high- k gate dielectrics shows that inclusion of these effects in the compact C-V model is necessary for accurate simulation of MOSFETs with high- k gate dielectrics.

Available at: http://teacher.buet.ac.bd/itrat/Itrat_TED_2007.pdf

- ◇ M. Itrat B. Shams et al. "Study of gate C-V characteristics of metal-oxide-semiconductor devices under uniaxial strain"

Journal: To be Submitted in Journal of Applied Physics

Abstract: Gate capacitance-voltage (C-V) characteristics of metal-oxide-semiconductor (MOS) devices on (100) Si substrate are studied theoretically under uniaxial strain along $\langle 110 \rangle$ direction. Stress levels up to 5 GPa (1.38% of strain) are considered for both n-type and p-type devices. From consideration of technological importance, nMOS devices under uniaxial tensile strain and pMOS devices under uniaxial compressive strain are investigated. C-V characteristics are simulated using a self consistent, quantum-mechanical model including wave function penetration effect. Changes in the hole effective masses and shifts of the different valence band edges due to strain are characterized as functions of the uniaxial stress, from the solution of the 6 band $k \cdot p$ hamiltonian. In addition to a flatband shift, strain is found to increase the gate capacitance under inversion bias and reduce the gate capacitance under accumulation bias for both type of devices. These effects can be explained in terms of strain induced shift of the band edges and changes in the effective masses, respectively. Experimentally observed larger enhancement of the drain current relative to the mobility enhancement in uniaxially strained devices are explained in terms of the increased inversion capacitance of the strained devices.

2. Md. Itrat Bin Shams et al. "Effects of Uniaxial Strain on the Gate Capacitance of Double Gate MOSFETs"

Conference: IEEE International Conference on Electron Devices and Solid-State Circuit 2008, Hong Kong

Abstract: Gate capacitance versus voltage (C-V) characteristics for double gate MOSFETs with uniaxially strained silicon substrate are presented incorporating wave function penetration effect. Changes in capacitance with stress levels up to 5 GPa are studied. Physical insights of the capacitance value change are also discussed. Contributions of band splitting and effective mass change in C-V due to uniaxial strain are analyzed. Dependencies of C-V change on doping density and body thickness for uniaxial strain are revealed for double gate MOSFETs.

Available at: http://teacher.buet.ac.bd/itrat/Itrat_EDSSC08.pdf

3. Md. Itrat Bin Shams et al. "An Improved Physically Based Compact C-V Model for MOS Devices with High-K Gate Dielectrics" **Best Student Paper Award**

Conference: International Conference on Electrical and Computer Engineering 2006, Dhaka, Bangladesh

Abstract: An improved compact gate C-V model for MOS devices with high-k gate dielectrics is proposed. The model accurately includes the effect of wave function penetration into the gate dielectric. It is based on making α , the exponent of the Airy function solution of the eigenenergy, dependent on the characteristics of the dielectric material and on the substrate doping density. Comparison with experimental C-V data shows that the proposed model is more accurate than existing model which consider a constant value of α for all dielectric materials and doping densities.

Available at: http://teacher.buet.ac.bd/itrat/Itrat_ICECE_2006.pdf

International Achievements

1. International Future Energy Challenge 2005

Citation: <http://www.energychallenge.org/>

Project Title: Utility Interactive Inverter System for Small Distributed Generation

Abstract: Renewable energy sources are becoming very popular all over the world as an alternate to the conventional one, made from natural resources (fossil fuels, etc.). So there is huge extent of works to be done in converting the variable DC voltage generated by sources like solar cells, etc. to a fixed DC and/or AC voltage. Our proposal of a utility interactive inverter system will prop up such works immensely. Here we have proposed a scheme, based on the use of conventional DC-DC converter, followed by a PWM inverter, for generating an output waveform having low Distortion Factor (DF). A constant output voltage is assured by varying the modulation index of the PWM pattern, which is fed to the gate of the inverter. The output voltage is synchronized with the grid voltage by using Phase-Locked Loop (PLL). Standalone operation is performed by detecting the abnormal grid condition. The scheme is tested both for 110V (50Hz) and 240V (60Hz) output. The efficiency is around 85% and hopefully it can be improved by identifying the components, where the loss is incurring.

Available at: http://teacher.buet.ac.bd/itrat/2005_Report_Final_BUET.pdf

2. IEEE Enterprise Award 2006

Citation: <http://www.ieee.org/organizations/foundation/2007news.html>

Project Title: Sustainable Technology Solutions for Providing ICT Based Services to Rural People

Abstract: To ensure sustainability of ICT dissemination initiatives among underprivileged rural people for improvement of livelihood, we propose research on solar photovoltaic solutions for powering ICT kiosks in off-grid villages, charging mobile phones for traveling infomediaries and Bengali interface for email/chatting for setting up communication between rural producers/vendors of products like handicrafts and distant potential buyers. Besides designing and developing these solutions, we will also implement and assess their sustainability using existing network. Our enterprise will contribute to current initiatives and help members appreciate professional responsibilities toward such global challenges.

3. Travel & subsistence grant to attend a research workshop, 2008

Workshop: EPEDC 2008 - Entrepreneurship for Physicist and Engineers from Developing Countries

Organizer: ICTP, International Center for Theoretical Physics

Venue: Kastler Lecture Hall, Trieste, Italy

Details: <http://teacher.buet.ac.bd/itrat/Achievements.html>