On the Physically Based Compact Gate C–V Model for Ultrathin Gate Dielectric MOS Devices Using the Modified Airy Function Approximation

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***Abstract*—The exponent (λ) of the modified Airy function solution of the quantized energy levels in the MOS potential well, which is used in the physically based quantum-mechanical compact gate C–V model of Li *et al.*, has been found to be dependent on the barrier height at the Si–dielectric interface and the substrate doping density. The physical origins of this dependence are discussed. An empirical equation that considers these effects is proposed for λ. Comparison with the experimental C–V data of MOS devices with high-k gate dielectrics shows that inclusion of these effects in the compact C–V model of Li *et al.* is necessary for the accurate simulation of MOS field-effect transistors with high-k gate dielectrics.**

***Index Terms*—Airy function approximation, compact C–V model, high-k gate dielectric, quantum-mechanical (QM) effect.**

I. Introduction

THE FEATURE sizes of MOS devices have entered the nanometer regime during the last few years. High-k materials are beginning to replace thin SiO_2 layers as gate dielectrics to overcome reliability and gate leakage current problems. Quantum-mechanical (QM) effects [2] are important in determining the gate C–V characteristics of such devices. Modeling of the QM effects becomes further complicated owing to the penetration of wave functions of the confined carriers into the gate dielectric. Extensive amount of work has been done to incorporate wave function penetration effect on gate C–V modeling [1], [3]–[6].

Compact C–V models that can take into account QM effects are attractive for everyday device and circuit studies. A physically based QM compact model has been proposed in [1]. Wave function penetration effect has been incorporated in this model by modifying the exponent (λ) of the Airy function solution for the quantized energy levels from the 2/3 power law. Li *et al.* [1] have proposed that λ for electrons and holes are independent of the properties of the gate dielectric materials. However, it is known that even for the same equivalent oxide thickness (EOT), gate capacitance depends on the properties of the gate dielectric materials due to the dependence of the wave function penetration effect on gate dielectrics [5], [6]. Therefore, it is not evident that the constant values of λ, as suggested in [1], would be applicable to devices with high-k gate dielectric materials.

In this paper, we investigate how variations in the wave function penetration, which are associated with different gate dielectrics, affect λ of the modified Airy function approximation. The effect of the substrate doping density on λ is also studied.

II. Theory

The infinite triangular potential approximation of the MOS potential well leads to the well-known Airy function solution for the quantized energy levels for electrons and holes, i.e.,

$$E_1 - E_{c,v} \cong \pm\gamma \left(\frac{|F_{\rm ox}|{\rm cm}}{\rm MV} \right)^{\lambda} \tag{1}$$

where γ is a constant depending on the quantization effective mass in Si m^*, and $\lambda = 2/3$. $F_{\rm ox}$ is the electric field in the gate dielectric at the Si–dielectric interface. The Airy function solution is inaccurate since the linear approximation of the potential profile in Si is not valid, and the wave function penetration effect is neglected. Li *et al.* have argued in [1] that the power law for E_1 remains valid even for realistic potential profiles considering wave function penetration. They have overcome the limitations of the Airy function solution by allowing the value of λ to vary from 2/3. By comparing with the results obtained from a self-consistent Schrödinger–Poisson solver including wave function penetration and assuming SiO_2 as the gate dielectric, it has been suggested in [1] that for electrons, $\lambda = 0.61$ and $\gamma = 77$ meV, and for holes, $\lambda = 0.64$ and $\gamma = 88$ meV.

In this paper, to include the variation of wave function penetration due to different gate dielectric materials, we allow λ to depend on the dielectric properties (namely dielectric constant k, dielectric effective mass $m^*_{\rm ox}$, EOT, and the barrier height at the Si–dielectric interface ϕ_b). Moreover, we also assume that λ may depend on the substrate doping density N (N_a for acceptor type and N_d for donor type). In order to investigate these effects, we numerically calculate E_1 for both electrons and holes using a self-consistent Schrödinger–Poisson solver

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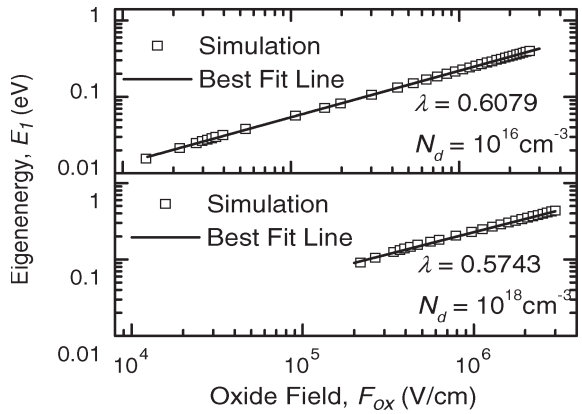

Fig. 1. E_1 versus $F_{\rm ox}$ for a pMOS with Y–O–Si gate dielectric for two different doping densities. λ is determined from the slope of the corresponding best fit line.

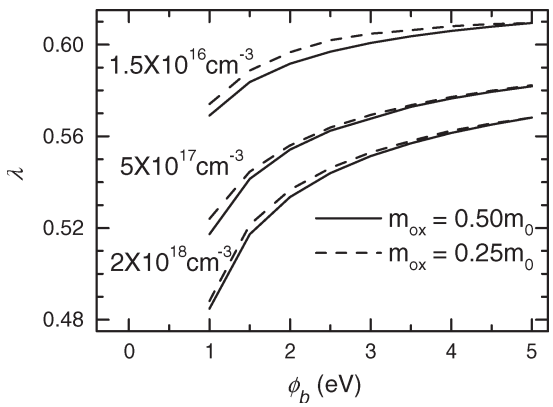

Fig. 2. λ versus ϕ_b of pMOS devices under inversion bias for two different values of $m_{\rm ox}$. Three different substrate doping densities are considered.

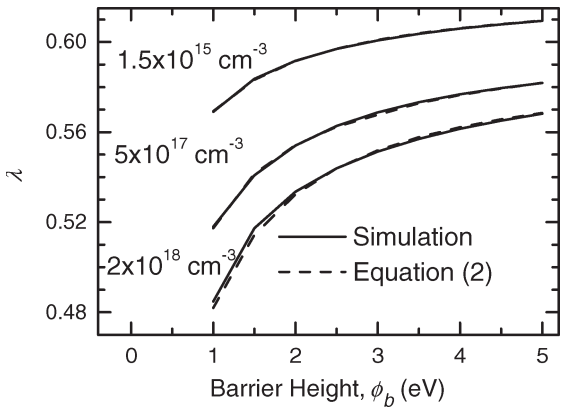

Fig. 3. Variation of λ with ϕ_b for different doping densities. Both numerically simulated results and empirical results obtained from (2) are shown.

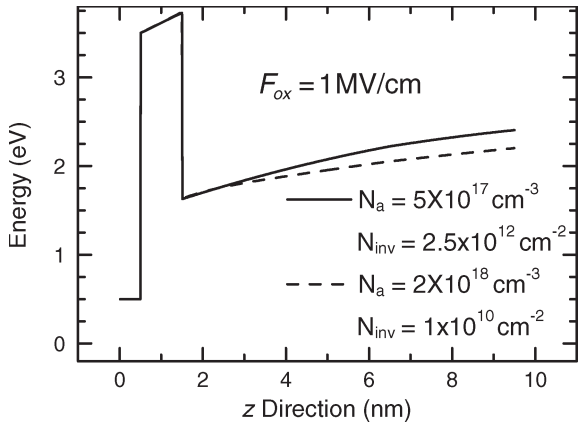

Fig. 4. Potential energy profiles of nMOS devices under inversion bias for two different N_a's. For both profiles, $F_{\rm ox} = 1$ MV/cm.

including wave function penetration effect [4], [5] and fit the numerical data with (1) to determine λ.

III. Results

Fig. 1 shows E_1 versus $F_{\rm ox}$, which were obtained from numerical simulations, for a pMOS device under inversion bias for two doping densities. Here, Y–O–Si is the gate dielectric with $\phi_b = 4.5$ eV [7], $m_{\rm ox} = 0.5m_0$, and EOT $= 1$ nm. It is found that the extracted values of λ indeed depend on the substrate doping density.

λ (which was extracted from numerical calculation) versus ϕ_b for pMOS devices under inversion bias condition for two different values of $m_{\rm ox}$ is presented in Fig. 2. Three different substrate doping densities are considered, and EOT $= 1$ nm. We observe that λ is not very sensitive to variations in $m_{\rm ox}$. We have also determined that while λ depends on ϕ_b and N, its dependence on EOT and k is rather weak. Therefore, in this paper, we neglect the variation of λ with $m_{\rm ox}$, EOT, and k.

Fig. 3 shows the calculated variation of λ with ϕ_b for pMOS devices with different substrate doping densities under inversion bias. We have considered $m_{\rm ox} = 0.5m_0$ and EOT $= 1$ nm. Similar results are also obtained for electrons (nMOS devices under inversion or pMOS devices under accumulation). It is observed that λ decreases with decreasing ϕ_b and increasing substrate doping density. When ϕ_b decreases, the penetration of the wave function into the gate dielectric increases. Consequently, the confinement of the carriers becomes less tight, and the eigenenergies are lowered. For a given $F_{\rm ox}$, a reduction in ϕ_b leads to a reduction in λ. The dependence of λ on N can easily be explained by considering the inversion bias. When N is increased while keeping $F_{\rm ox}$ fixed, the inversion carrier density $N_{\rm inv}$ is reduced due to an increase in the depletion charge density. Therefore, the same $F_{\rm ox}$ gives two different potential profiles for two different N's. This situation is illustrated in Fig. 4 for nMOS devices under inversion bias. When N is higher, the potential well is wider and shallower, which lowers the eigenenergies. In Fig. 4, for $F_{\rm ox} = 1$ MV/cm, the lowest eigenenergy E_1 relative to the bottom of the potential well is 132.1 meV for $N_a = 5 \times 10^{17}$ cm^{-3} and 127.4 meV for $N_a = 2 \times 10^{18}$ cm^{-3}. This explains the substrate doping density dependence of λ.

We propose that the dependence of λ on ϕ_b and N may be expressed by the following empirical bilinear relationship:

$$\lambda = \frac{P_1\phi_b + P_2}{\phi_b + P_3} \tag{2}$$

TABLE I
COEFFICIENTS OF (3)–(5) FOR ELECTRONS AND HOLES. HERE, "E" REPRESENTS ELECTRONS, AND "H" REPRESENTS HOLES

		P_{i5}	P_{i4}	P_{i3}	P_{i2}	P_{i1}	P_{i0}
P_1	e	-5.005×10^{-5}	0.0018148	-0.0197407	0.072722	-0.07048	0.6391
	h	-8.1362×10^{-5}	0.00294612	-0.031948	0.11673	- 0.108347	0.06338
P_2	e	-9.755×10^{-5}	0.00358048	-0.039882	0.15386	-0.1683	0.04982
	h	-0.0010917	0.03941614	-0.524591	1.52233917	-1.283078	0.3197
P_3	e	-6.1225×10^{-5}	0.00230055	-0.02676054	0.11142	-0.1431	0.1184
	h	-0.001635424	0.059014	0.63485	2.2672	-1.867476	0.06223

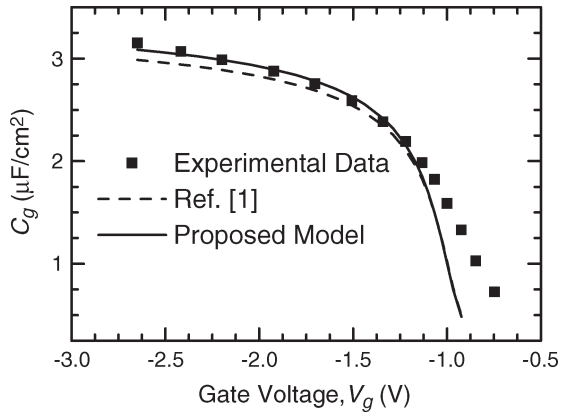

Fig. 5. Accumulation C–V characteristics of a nMOS device with nitrided ZrO_2 gate dielectric. Experimental data are taken from [8].

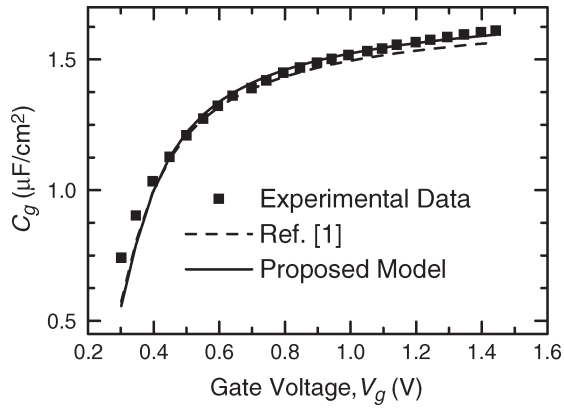

Fig. 6. Accumulation C–V characteristics of a pMOS device with HfO_2 gate dielectric. Experimental data are taken from [9].

where

$$P_1 = P_{15}N_n^5 + P_{14}N_n^4 + P_{13}N_n^3 + P_{12}N_n^2 + P_{11}N_n + P_{10} \quad (3)$$

$$P_2 = P_{25}N_n^5 + P_{24}N_n^4 + P_{23}N_n^3 + P_{22}N_n^2 + P_{21}N_n + P_{20} \quad (4)$$

$$P_3 = P_{35}N_n^5 + P_{34}N_n^4 + P_{33}N_n^3 + P_{32}N_n^2 + P_{31}N_n + P_{30}. \quad (5)$$

However, we do not assign any physical significance to the particular functional form of (2). Here, $N_n = N(\mathrm{cm}^{-3})/10^{17}$.

The values of the coefficients of (3)–(5) for electrons and holes are obtained by comparing with the numerical results and are given in Table I.

Next, we investigate the improvement that may be achieved in simulating the gate C–V characteristics of MOS structures with high-k gate dielectrics by using (2) and Table I for λ instead of the constant values given in [1]. Fig. 5 shows the experimental high-frequency C–V under accumulation bias of an nMOS device with nitrided ZrO_2 as the gate dielectric. The data are taken from [8]. Holes are the confined carriers for this bias. The simulated C–V using the proposed model ($\lambda = 0.60$) as well as the constant value of λ [1] is also shown. Various device parameters are taken from [6] and are listed as follows: $N_a = 2.1 \times 10^{15}$ cm^{-3}, $\phi_b = 1.8$ eV, EOT $= 0.88$ nm, and $V_{\mathrm{FB}} = -0.8$ V. It is observed that when the N and ϕ_b dependences of λ are taken into account, the simulation becomes more accurate. The error relative to the experimental data in strong accumulation is 5% for the model of Li *et al.* [1] and 2% for the proposed model. The experimental high-frequency C–V of a pMOS device under accumulation bias with HfO_2 gate dielectric is presented in Fig. 6. The data are taken from [9]. Electrons are the confined carriers for this bias. N_d, EOT, and V_{FB}, which were extracted from the experimental data, are found to be 2×10^{18} cm^{-3}, 1.87 nm, and 0.35 V, respectively, and $\phi_b = 1.5$ eV [7]. Simulated C–V's are also shown calculated using (2) ($\lambda = 0.57$) and a constant value for λ. The error in strong accumulation is 3% for the model of [1] and 1% for the proposed model. Again, it is seen that for accurate simulation, it is necessary to include the ϕ_b and N dependence of λ in the model. In both Figs. 5 and 6, it is observed that the use of constant values of λ from [1] leads to an

underestimation of the slope of the C–V characteristics under high gate bias voltages. The slope is important for extracting EOT and other parameters [6]. The underestimation of the C–V slope is caused by an overestimation of the eigenenergies through using higher values of λ in [1]. Equation (2) provides an easy way of improving the accuracy of the QM compact gate C–V model of Li *et al.* [1] by incorporating the ϕ_b and N dependence of λ.

IV. Conclusion

We have investigated the dependence of λ, i.e., the modified exponent of the Airy function solution of the quantized energy levels, on the barrier height at the Si–dielectric interface ϕ_b and the substrate doping density N. An empirical expression is proposed to describe this dependence. We have also presented physically based arguments to explain the dependence of λ on ϕ_b and N. It is shown that when these effects are taken into account, simulation of the C–V characteristics of MOS devices with high-k gate dielectrics using the physically based QM compact model of [1] becomes more accurate.

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