IMPROVED COMPACT GATE C-V MODEL FOR ULTRATHIN HIGH-k DIELECTRICS

A thesis submitted for the partial fulfillment of the requirement

of the degree of

Bachelor of Science

By

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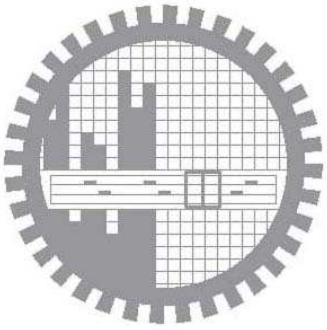

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October, 2006

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Certification

The thesis titled **"Improved compact gate C-V model for ultrathin high-k dielectrics"** submitted by Md. Itrat Bin Shams (0006026), K. M. Masum Habib (0006012) and Rajib Mikail (0006065), session _____, has been accepted satisfactory in partial fulfillment of the requirement for the degree of *Bachelor of Science in Electrical and Electronic Engineering* on _____,2006.

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Declaration

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Acknowledgements

We would like to thank Dr. Quazi Deen Mohd Khosru, Professor, Department of Electrical and Electronic Engineering (EEE), Bangladesh University of Engineering and Technology (BUET), Dhaka, our supervisor, for his many suggestions and constant support during this research.

We are also grateful to Dr. Anisul Haque, Professor Department of Electrical and Electronic Engineering, East West University, Bangladesh, our former supervisor, for his constant guidance, supervision, and constructive suggestions, without which this work could not be done.

We would like to thank the head of the department of Electrical and Electronic Engineering for everything he did for us.

We are grateful to A. N. M Zainuddin, former Lecturer, Department of EEE, BUET, Dhaka, for his continuous motivation and help.

We also want to thank A. E. Islam, former Lecturer, Department of EEE, BUET, Dhaka for his suggestions and support.

Finally, we wish to thank Asif I. Khan for many fruitful discussions and Mr. Shafayet, Lab Attendant, Robert Noyce Simulation Lab for his support.

BUET, Dhaka, Authors

October, 2006

Abstract

An improved compact gate capacitance-voltage (C-V) model for MOS devices with high-k gate dielectrics is proposed. In this model the effects of characteristics of dielectric material and substrate doping density are accurately included. It also includes the effects of wave function penetration into the gate dielectric. It is based on making λ, the modified exponent of the 2/3 power law relationship ($E_1 \propto F_{ox}^{2/3}$) for the first eigenenergy, dependent on the characteristics of the dielectric material and on the substrate doping density. The effects of wave function penetration is included by extracting λ from self-consistent solutions of coupled Schrödinger-Poisson equation for eigenenergies. It is observed that λ strongly depends on barrier height and substrate doping density and that factors such as dielectric constant (k) of gate dielectric material, effective masses of holes and electrons, effective oxide thickness (EOT), work function of gate metal and existence of metal or polysilicon as gate, have negligible effect on λ. An empirical relationship is proposed to represent λ as a function of barrier height and substrate doping density both for holes and electrons. It is found that λ increases with the increment in barrier height and λ decreases with the increment in doping density. Comparison with experimental C-V data shows that the proposed model is more accurate than existing model where λ was considered to be independent of characteristics of dielectric materials and doping densities.

Chapter 1

Introduction

Within past few years, aggressive scaling down of MOS devices has been continued and the feature sizes of MOS devices have entered in nanometer regime. Throughout the history of integrated circuit (IC) design, a general scaling methodology has been employed [1]. As guided by the International Technology Roadmap for Semiconductors (ITRS), the scaling down has been accomplished by a decrease in gate-oxide thickness and increase in doping density.

As the feature sizes go into nanometer regime, a very large electric field normal to the Si/SiO_2 interface is observed even near the threshold of inversion. This leads to significant bending of the energy band. With significant band bending, the potential well can become sufficiently narrow to quantize the carriers. Due to the quantization of energies of inversion carriers in potential well, the distribution of the carriers can no longer be represented by semi-classical models [2, 3], rather quantum mechanical (QM) models must be used [4].

When the gate oxide thickness becomes less than 2 nm, a substantial current flows through gate-oxide due to direct tunneling. In order to decrease this current, and to overcome the serious technology difficulties related to using ultra-thin SiO_2 layers as the gate dielectric, alternative high-k materials are being considered as replacement [1] since for a given EOT, high-k dielectrics offers greater physical thickness than SiO_2 and hence less tunneling current [5].

It has been shown that the wave function penetration effect has to be considered for proper simulation of C-V characteristics of MOS devices especially for high-k gate dielectrics [6, 7]. Recently, extensive amount of work has been done to incorporate QM effects on C-V characteristics of ultra-thin MOS devices [8, 9]. And many self-consistent numerical simulators have been developed to simulate C-V characteristics accurately [10]. However, computationally efficient analytic compact models are preferred for practical everyday circuit and device studies. In order to solve this problem, Li et al. presented a physically based compact model to calculate C-V characteristics for ultra-thin gate dielectrics [11]. For sake of compactness of the model in Ref. [11], the authors did not calculate the eigenenergies self-consistently. Instead, they used a modified value for the exponent over oxide field of the 2/3 power law relationship ($E_1 \propto F_{ox}^{2/3}$) to calculate the lowest quantized energy level. And the exponent, called λ, was extracted from self-consistent simulation results of a MOS device with SiO_2 as gate-dielectric material. The value of λ extracted in this way was showed to be independent of substrate doping density. It was assumed that this calculated value of λ would be reliable for high-k gate MOS devices especially, when high-k gate stacks are employed with a thin layer of SiO_2 incorporated adjacent to the interface. The use of the model for high-k gate MOS devices with different substrate doping density is not justified.

1.1 Literature Review

Two important phenomenon, that have to be considered for accurate modeling of ultra-thin gate oxide MOSFETs, are quantization and wave-function penetration. Significant amount of works have been done on these matters. However, analytic compact models are preferred for practical everyday circuit and device studies. So, a lot of compact models are also developed.

Mudanai et al. [8] has proposed a model to understand wave function penetration in NMOS inversion region of capacitance voltage characteristics. Their study revealed that wave function penetration into the gate dielectric causes carrier profile to be shifted closer to the gate dielectric reducing the electrical oxide thickness. As a result of this

C-V curve shows different result from conventional simulator results.

Haque et al. [12] calculated normalized wave-functions in one dimensional well structure. It is a technique to calculate: (i) the eigenenergies and the normalized eigenstates in quantum wells, (ii) the energy broadened spatially varying density-of-states in leaky quantum wells where the particle lifetime is finite, and (iii) the energy position dependent density-of-states in quantum wells where phase-breaking and/or inelastic scattering processes are present. The method is based on the Greens function formalism. Hareland [13] showed another approach for estimation of quantized energy in quantum wells for hole inversion layer. This implies the implementation and results of a simple, computationally efficient model, appropriate for device simulators, for predicting the effects of hole inversion layer quantization.

Moglestue presented a self-consistent calculation for electron and hole inversion [14]. Charge distribution has been calculated by solving Schrödinger and Poisson's equation. In strong inversion deviation of C-V curves from that with triangular well approximation, is observed. Jimėnez showed a compact model based on the Landauer transmission theory for the silicon quantum wire and quantum well metal oxide semiconductor field effect transistor MOSFET, that is working in the ballistic limit [15]. Liu et al. [16] also presented a compact model Considering the Finite Charge Layer Thickness. But here only quantization effect is considered. No wave-function penetration is taken into account. This model captures the static current-voltage characteristics in all the operation regions, below and above threshold voltage. A model to calculate gate-capacitance incorporating wave-function penetration is presented by Hakim et al. in [6]. It is shown that C-V curves are independent of dielectric material if wave-function penetration is not considered. It is seen that calculated gate capacitance is higher for materials with lower conduction band offsets with silicon. They have investigated the effects of substrate doping density on the relative error in gate capacitance in case of no wave function penetration consideration. It is found that the error decreases with increasing doping density.

Rahman et al. [17] presented a model via which broadening of quantized inversion layer states is shown in deep submicron MOSFETs. This is needed for accurate mod-

eling of ultrathin gate oxide dielectric C-V. Again Haque et al. [18] calculated the normalized electron wave functions in the inversion layers of nMOSFETs with ultra-thin gate oxides using an asymptotic boundary condition that considers flat energy band profile deep inside the metal as well as deep inside the semiconductor. They showed that the use of the conventional boundary condition overestimates the distance of the carriers from the interface by a few angstroms.

All these literatures are used to build improved compact model and self-consistent model used in the improved compact model.

1.2 Objective of This Work

As mentioned earlier, in the model proposed by Li et al. [11], λ was considered to be independent of the dielectric material characteristics and substrate doping density. Hence, the use of the model for MOS devices consisting of different high-k gates and different substrate doping densities is not justified. To justify this, in our study, we have assumed λ to be a function of characteristics of dielectric materials such as dielectric constant (k), effective mass (m^*), barrier height (ϕ_b), gate metal characteristics such as metal work function (ϕ_m), and substrate doping density ($N_{a,d}$) to propose an improved compact C-V model, i.e.,

$$\lambda = f(\phi_b, N_{a,d}, k, m^*, \phi_m) \tag{1.1}$$

In order to determine function 1.1, we have used a self-consistent simulator. This simulator uses Green's function formalism and considers wave-function penetration into the gate dielectric material [9]. Accurate modeling of gate capacitance is possible via this simulator. Several simulations were done for different materials with different doping concentrations with different gate metals. From these simulations, 1.1 was determined.

1.3 Organization of The Thesis

In chapter 2 necessary theories to develop self-consistent model and compact model is given. Methods to calculate effective oxide thickness and flat-band voltage as well as doping density of bulk silicon is also given. Detailed calculation of exponent value determination is stated in chapter 3. Comparison of simulated C-V generated from compact model and revised compact model with experimental data is also presented there. Error curves are provided to show the validity of our model. Flowchart of our model and self-consistent model are given in appendix section.

Chapter 2

Theory

This chapter describes theories used to produce improved compact model. The self-consistent calculations will be presented, followed by the compact model of Ref [11] and finally proposed improved compact model will be presented. Basic MOS structure and its operation is given first.

2.1 MOSFET Basics

One of the most widely used electronic devices, particularly in digital integrated circuits, is the *metal-insulator-semiconductor (MIS)* transistor. Most such devices are made using silicon as the semiconductor, SiO_2 as the insulator, and metal or heavily doped poly crystalline silicon, also known as polysilicon, as the gate electrode. The term *metal oxide semiconductor field-effect transistor (MOSFET)* is commonly used to refer this devices.

In this section, basic theories for understanding a MOSFET will be discussed. A brief discussion on structure and operation of enhancement type n-MOSFET is given first which is followed by the band structure under flat-band, inversion and accumulation condition. Finally, a discussion on a typical C-V curve explaining different operating conditions is provided.

2.1.1 MOS Structure

Let us consider the n-channel enhancement-type transistor shown in Fig. 2.1. The transistor is fabricated on a p-type substrate, which is a single-crystal silicon wafer that provides physical support for the device (and for the entire circuit in the case of an integrated circuit). Two heavily doped n-type regions, indicated in the figure as the n^+ **source** and n^+ **drain** regions, are created in the substrate. A thin layer of silicon dioxide (SiO_2), which is an excellent electrical insulator, is grown on the surface of the substrate, covering the area between the source and drain regions. Metal is deposited on top of the oxide layer to form the **gate electrode** of the device. Metal contacts are also made to the source region, the drain region, and the substrate also known as the **body**. Thus, four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

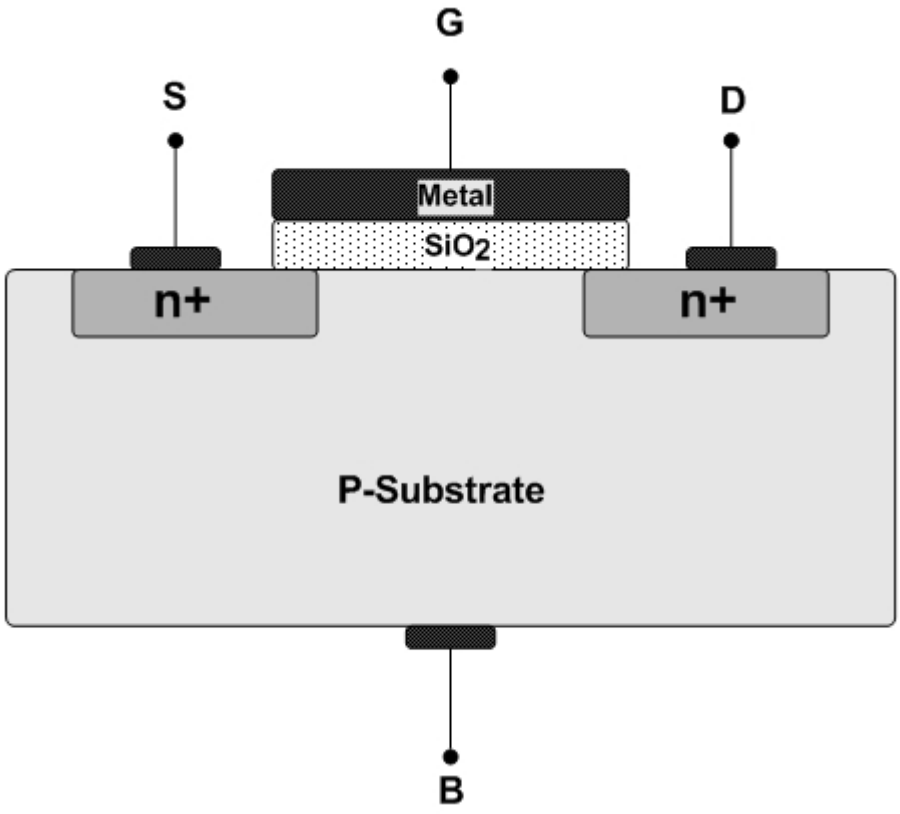

Figure 2.1: Cross section of an enhancement-type n-MOSFET.

2.1.2 MOS Operation

Operation with No Gate Voltage

With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the $p-n$ junction between the n^+ drain region and the p-type substrate, and the other diode is formed by the $p-n$ junction between the p-type substrate and the n^+ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage v_{DS} is applied. In fact, the path between drain and source has a very high resistance (of the order of $10^{12}\Omega$).

Creating a Channel for Current Flow

Let us consider the source and the drain are grounded and a positive voltage is applied to the gate. The positive voltage on the gate causes, in the first instance, the free holes (which are positively charged) to be repelled from the region of the substrate under the gate (the channel region). These holes are pushed downward into the substrate, leaving behind a carrier-depletion region. The depletion region is populated by the bound negative charge associated with the acceptor atoms. These charges are "uncovered" because the neutralizing holes have been pushed downward into the substrate.

The positive gate voltage attracts electrons from the n^+ source and drain regions (where they are in abundance) into the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an n region is in effect created, connecting the source and drain regions. Now if a voltage is applied between drain and source, current flows through this induced n region, carried by the mobile electrons. The *induced* n region thus forms a channel for current flow from drain to source. Correspondingly, the MOSFET is called an **n-channel** MOSFET or, alternatively, an **n-MOS** transistor. Here the n-channel MOSFET is formed in a p-type substrate. The channel is created by *inverting* the substrate surface from p type to n type. Hence the induced channel is also called an **inversion layer**.

The gate and body of the MOSFET form a parallel-plate capacitor with the oxide layer acting as the capacitor dielectric. The positive gate voltage causes positive charge to accumulate on the top plate of the capacitor (the gate electrode). The corresponding negative charge on the bottom plate is formed by the electrons in the induced channel. An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, thus it determines the channel conductivity and, in turn, the current that will flow through the channel when a voltage v_{DS} is applied. Current is carried by free electrons traveling from source to drain *(hence the names source and drain)*.

The value of v_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage and is denoted V_t. As v_{GS} exceeds V_t, more electrons are attracted into the channel. We may visualize the increase in charge carriers in the channel as an increase in the channel depth. The result is a channel of increased conductance or, equivalently, reduced resistance. In fact, the conductance of the channel is proportional to the excess gate voltage ($v_{GS} - V_t$), also known as the effective voltage. It follows that the current i_D will be proportional to ($v_{GS} - V_t$) and, of course, to the voltage v_{DS} that causes i_D to flow.

As we travel along the channel from source to drain, the voltage (measured relative to the source) increases from 0 to v_{DS}. Thus the voltage between the gate and points along the channel decreases from v_{GS} at the source end to $v_{GS} - v_{DS}$ at the drain end. Since the channel depth depends on this voltage, we find that the channel is no longer of uniform depth; rather being deepest at the source end and shallowest at the drain end. When v_{DS} is increased to the value that reduces the voltage between gate and channel at the drain end to V_t the channel depth at the drain end decreases to almost zero, and the channel is said to be **pinched off**. Increasing v_{DS} beyond this value causes the pinch off point to move along to source. The voltage across the channel from source to pinch off point becomes constant with the increasing v_{DS}. Hence the drain current **saturates**.

2.1.3 Band Diagram

To explain the operation of a MOSFET it is customary to define a modified work function $q\Phi_m$ used to measure the energy from the metal Fermi level to the conduction band of the oxide. Similarly, $q\Phi_s$ is the modified work function at the semiconductor-oxide interface. Now if we apply a negative voltage between the metal and the semiconductor, we effectively deposit a negative charge on the metal. In response, we expect an equal net positive charge to accumulate at the surface of the semiconductor. In the case of a p-type substrate this occurs by **hole accumulation** at the semiconductor-oxide interface. Since the applied negative voltage *depresses* the electrostatic potential of the metal relative to the semiconductor, the electron energies are *raised* in the metal relative to the semiconductor. As a result, the Fermi level for the metal E_{Fm} lies above its equilibrium position by qV, where V is the applied voltage.

Since $q\Phi_m$ and $q\Phi_s$ do not change with applied voltage, moving E_{Fm} up in energy relative to E_{Fs} causes a tilt in the oxide conduction band. The energy bands of the semiconductor *bend* near the interface to accommodate the accumulation of holes. Here the Fermi level near the interface lies closer to the valance band, indicating a larger hole concentration than that arising from the doping of the p-type semiconductor. The energy band diagram of an n-MOSFET in accumulation is shown in Fig. 2.2.

Applying positive voltage from the metal to the semiconductor raises the potential of the metal, lowering the metal Fermi level by qV relative to its equilibrium position. As a result, the oxide conduction band is again tilted. The positive voltage deposits positive charge on the metal and calls for a corresponding net negative charge at the surface of the semiconductor. Such a negative charge in p-type material arises from **depletion of holes** from the region near the surface, leaving behind *uncompensated ionized acceptors*. This is analogous to the depletion region at a $p-n$ junction. In the depleted region the hole concentration decreases, moving E_i closer to E_F and *bending* the bands down near the semiconductor surface. The energy band diagram of an n-MOSFET in depletion is shown in Fig. 2.3.

If we continue to increase the positive voltage, the bands at the semiconductor surface bend down more strongly. In fact, a sufficiently large voltage can bend E_i *below* E_F.

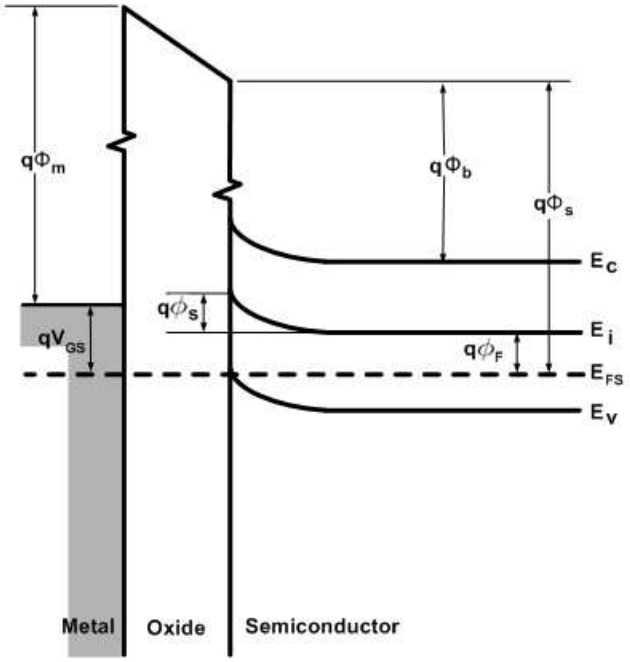

Figure 2.2: Energy band diagram of an enhancement-type n-MOSFET in accumulation.

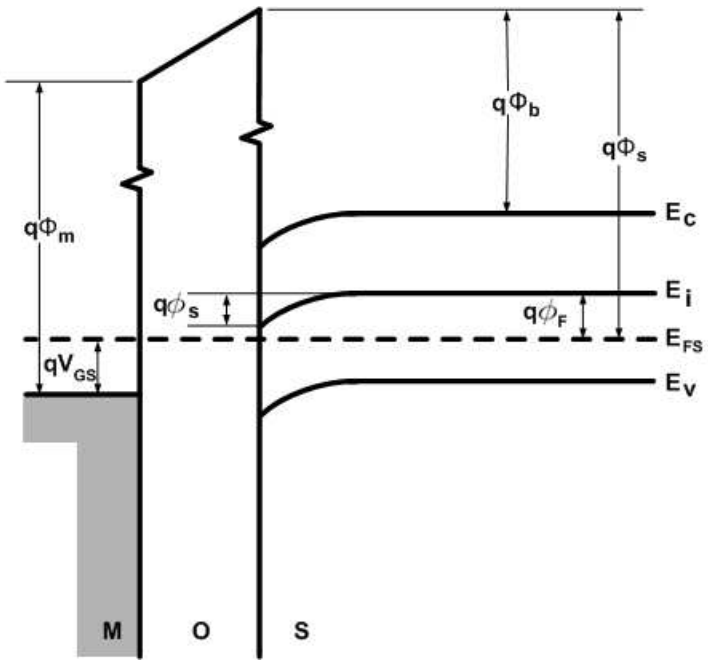

Figure 2.3: Energy band diagram of an enhancement-type n-MOSFET in depletion.

Here $E_F \gg E_i$ implies a large electron concentration in the conduction band. The region near the semiconductor surface in this case has conduction properties typical of n-type material. This n-type surface layer is formed not by doping, but instead by **inversion** of the originally p-type semiconductor due to the applied voltage. We define

a potential ϕ at any point measured relative to the equilibrium position of E_i. The energy $q\phi$ tells us the extent of band bending and $q\phi_s$ represents the band bending at the surface. At the **flat band** condition $\phi_s = 0$. When $\phi_s < 0$, the bands bend up at the surface, and we have hole accumulation. Similarly, when $\phi_s > 0$, we have depletion. Finally, when ϕ_s is positive and larger than ϕ_F, the bands at the surface are bent down such that E_i lies below E_F, and inversion is obtained. For strong inversion the surface should be as strongly n-type as the substrate is p-type. That is, E_i should lie as far below E_F at the surface as it is above E_F far from the surface. This condition occurs when $\phi_s(inv.) = 2\phi_F$.

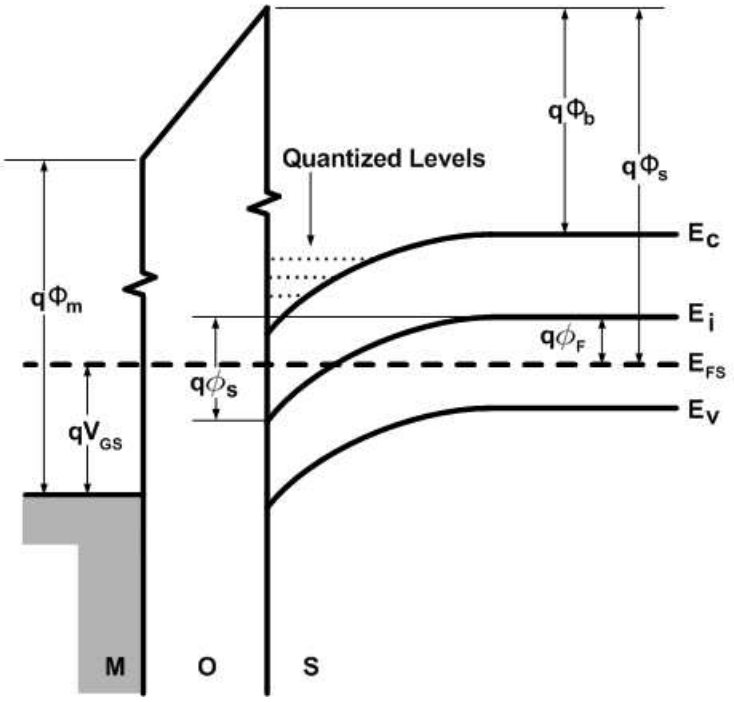

Figure 2.4: Energy band diagram of an enhancement-type n-MOSFET in strong inversion.

As shown in Fig. 2.4, the significant amount of band bending forms a potential well. And the potential well may become narrow enough to split the energy of the carrier under strong inversion. Due to the quantization of energies of inversion carriers in potential well, the distribution of the carriers can no longer be represented by semi-classical models [2, 3], rather quantum mechanical (QM) models must be used [4] as shown in Fig. 2.5.

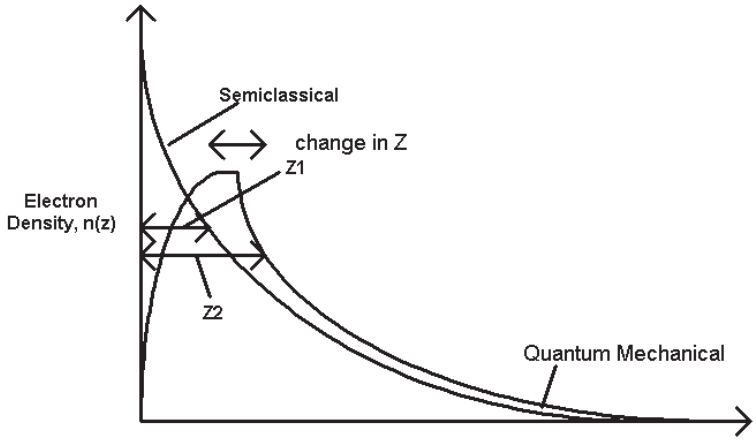

Figure 2.5: Electron distribution in the inversion layer of an n-MOSFET.

2.1.4 Gate Capacitance

The C-V characteristics of the MOS structure vary depending on whether the semiconductor surface is in accumulation, depletion, or inversion as shown in Fig. 2.6. The electrical equivalent of MOS capacitor is the series combination of a fixed voltage-independent gate insulator capacitance and a voltage-dependent semiconductor capacitance, such that the overall MOS capacitance becomes voltage dependent.

The series capacitance in accumulation is basically the insulator capacitance, C_i. Since, for negative voltage, holes are accumulated at the surface, the MOS structure appears almost like a parallel-plate capacitor, dominated by the insulator properties. As the voltage becomes less negative, the semiconductor surface is depleted. The depletion layer capacitance C_d, added in series with C_i, decreases until finally inversion is reached. After inversion is reached, the small signal capacitance depends on whether the measurements are made at high or low frequency, where "high" and "low" are with respect to the generation-recombination rate of the minority carriers in the inversion layer. If the gate voltage is varied rapidly, the charge in the inversion layer cannot change in response, and thus does not contribute to the small signal a-c capacitance. Hence, the semiconductor capacitance is at a minimum, corresponding to a minimum depletion width.

On the other hand, if the gate bias is changed slowly, there is time for minority carriers

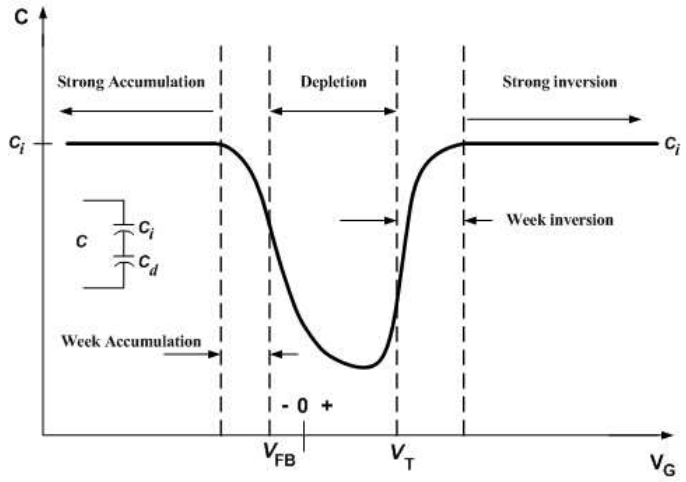

Figure 2.6: Semi-classical C-V characteristics of an enhancement-type n-MOS.

to be generated in the bulk, drift across the depletion region to the inversion layer, or go back to the substrate and recombine. Now the semiconductor capacitance is very large because the inversion charge increases exponentially with ϕ_s. Hence the low frequency MOS capacitance in strong inversion is basically C_i once again. In accumulation we get a very high capacitance both at low and high frequencies because the majority carriers in the accumulation layer can respond much faster than minority carriers.

2.2 Self Consistent Solution

Self-consistent simulator is used to get the value of exponent λ over oxide field to calculate first eigenstate. In our improved compact model this λ varies with barrier height and doping density. So simulation is performed for different materials with different doping densities for gate dielectric. The self consistent simulator used here is based on Green's function formalization [9]. Total calculation is given below for it.

2.2.1 Model

Self-consistent solution of coupled Schrödinger and Poisson's equation as proposed by Stern [4] and Moglestue [14] is presented here. Three major assumptions by stern

are,

(1) effective mass approximation is valid. So periodic potential need not be taken into account.

(2) At the silicon surface envelop wavefunction vanishes.

(3) Surface states are neglected and any charge in the oxide near semiconductor body can be replaced by an electric field.

Within the effective mass approximation, Schrödinger's equation for the wave function $\psi_{0_{ij}}$ can be written as,

$$[-\frac{1}{2}\hbar^2\nabla m^{*-1}\nabla + eV(z)]\psi_{0_{ij}} = E'_{ij}\psi_{0_{ij}} \tag{2.1}$$

where, m^{*-1} is the effective mass tensor, $V(z)$ the electrostatic potential, e is the magnitude of electron charge and E'_{ij} is the energy. z is taken to be positive inside the semiconductor.

According to Stern [4], the electronic wavefunction $\psi_{0_{ij}}$ for the jth subband in the ith valley can be expressed in terms of Bloch function traveling parallel to the interface, constrained by an envelope function normal to it. So,

$$\psi_{0_{ij}}(x, y, z) = \psi_{ij}(z)e^{i\theta z}e^{ik_x x + ik_y y} \tag{2.2}$$

where, k_x and k_y represents the transverse component of the wave vector k of the electron measured relative to the band edge. θ depends on k_x and k_y. Envelope function $\psi_{ij}(z)$ is the solution of,

$$[-\frac{\hbar^2}{2m_{zi}}\frac{d^2}{dz^2} + eV(z)]\psi_{ij}(z) = E_{ij}\psi_{ij}(z) \tag{2.3}$$

where, m_{zi} is the effective mass perpendicular to the interface and E_{ij} is the eigenenergy of the jth subband in the ith valley in the same direction.

Boundary conditions commonly used for the solution of (2.3) are $\psi_{ij}(\infty) = 0$ deep inside the semiconductor and at the oxide semiconductor interface, $\psi_{ij}(0) = 0$. Each eigenvalue E_{ij} found from the solution of Eq. (2.3) is the bottom of subband, with energy levels given by,

$$E_{ij}^{'} = E_{ij} + \hbar^2 k_x^2/2m_x + \hbar^2 k_y^2/2m_y \tag{2.4}$$

here m_x and m_y are the principal effective masses for motion parallel to the surface. Because the conduction band of silicon has six ellipsoidal valleys along the [100] direction of the Brillouin zone, there can be as many as three values of m_z depending on the surface orientation. In the effective mass approximation , the valleys are degenerate in pairs. Thus solution of Eq. (2.3) gives the eigenenergy E_{ij} and the envelope function $\psi_{ij}(z)$.

The potential $V(z)$ is found from the solution of Poisson's equation,

$$\frac{d^2V(z)}{dz^2} = -\frac{[\rho_{depl}(z) - \epsilon \sum_{ij} N_{ij}|\psi_{ij}(z)|^2]}{\epsilon_{si}\epsilon_0} \tag{2.5}$$

where, ϵ_{si} is the dielectric constant of semiconductor, N_{ij} is the carrier concentration of the jth subband in the ith valley. N_{ij} is given by the following equation,

$$N_{ij} = \frac{n_{vi} m_{di} kT}{\pi\hbar^2} \ln[1 + \exp(\frac{E_F - E_{ij}}{kT})] \tag{2.6}$$

where, n_{vi} is the valley degeneracy and m_{di} is the density of states effective mass of the ith valley given by $m_{di} = \sqrt{m_{xi} m_{yi}}$. E_F is the fermi energy.

$\rho_{depl}(z)$ is the charge density in the depletion layer, which is taken to be,

$$\rho_{depl}(z) = \begin{cases} -e(N_A - N_D), & 0 < z < z_d \\ 0, & z > z_d \end{cases} \tag{2.7}$$

here, z_d is the depletion layer thickness given by,

$$z_d = \sqrt{\frac{2\epsilon_{si}\epsilon_0\Phi_d}{e(N_A - N_D)}} \tag{2.8}$$

where Φ_d is the band bending due to depletion charge only. Φ_d can be calculated as,

$$\Phi_d = \Phi_s - \frac{kT}{e} - \frac{eN_{inv}z_{avg}}{\epsilon_{si}\epsilon_0} \tag{2.9}$$

Here, Φ_s is the total band bending, N_{inv} is the total number of charges per unit area in the inversion layer given by,

$$N_{inv} = \sum_{ij} N_{ij} \tag{2.10}$$

and z_{avg} is the average penetration of the inversion charge density into silicon given by,

$$z_{avg} = (1/N_{inv}) \sum_{ij} N_{ij} \int z|\psi_{ij}|^2 dz \tag{2.11}$$

The two boundary conditions necessary for the solution of Eq. (2.5) are $\frac{dV}{dz} = 0$ for large z and at the surface, its value is -F_s, where,

$$F_s = \frac{e(N_{inv} + N_{depl})}{\epsilon_{si}\epsilon_0} \tag{2.12}$$

is the surface electric field in silicon, and

$$N_{depl} = z_d(N_A - N_D) \tag{2.13}$$

is the number of charge per unit area in the depletion layer.

2.2.2 Calculation

The self-consistent solution starts with a initial estimate of potential $V(z)$ and then solve (2.3) and (2.5) iteratively until input potential from (2.5) matches with (2.3) within reasonable limits.

A typical method can be to replace $V(z)$ with -F_sz for $z > 0$ and with infinite barrier height for $z < 0$. This is shown in [4]. But this approximation is valid for low level of inversion charges.

If all the carriers are considered to be in the lowest subband then the initial assumption of $V(z)$ can be found from variational approximation. For this trial eigenenergies for the initial solution can be obtained by the variational technique described in [4]. But it is valid in low temperature. At high temperature all the carriers do not stay in the lowest subband. In this case we should start with the smaller value of N_{inv} and gradually increase this value. In each case last potential is the starting approximation of last. After solving Eq. (2.3) for ψ_{ij} and E_{ij} with the approximate equation, the fermi energy, E_F can be found from Eq. (2.6) and (2.10) for a given N_{inv}. When the fermi energy is known, N_{ij} for every subband can be obtained from (2.6).

The potential thus obtained by solving Poisson's equation with the boundary conditions stated above. The potential is then used in Schrödinger's equation to get values of E_F and E_{ij} for all subbands Poisson's equation is solved again and this procedure is continued until the energy converges.

The convergence of result means that successive eigenenergy values do not have difference more than 10^{-6} eV. Also successive potential values have to be placed within $KT/2000, (E_F - E_0)/10^4$ or 10^{-6} eV. E_F must also converge as it is the most important parameter in this calculation.

2.2.3 Green's Function Formalism

Green's function is a technique that helps to find any quantity that is initiated by an excitation at other point. For MOS devices retarded Green's function for the i'th valley at any distance z is given by,

$$[E + \frac{\hbar^2}{2m_{zi}}\frac{\partial^2}{\partial z^2} - eV(z) + i\epsilon]G_i^R(z, z^{'}; E) = \delta(z - z^{'}) \tag{2.14}$$

where ϵ is an infinitesimally small positive energy. Retarded Green's function $G_i^R(z, z^{'}; E)$ can be considered as a wave function at z originated by an excitation at z'. But Green's function is continuous at $z = z'$ and its derivative is discontinuous at z' by, $2m_{zi}/\hbar^2$.

G_i^R is used to calculate the one dimensional density of states, N_{1D}, eigenenergies E_{ij} and normalized wavefunctions, ψ_{ij}. The logarithmic derivative of the retarded Green's function G^R is defined by,

$$Z_i(z, z'; E) = \frac{2\hbar}{im_{zi}}[\frac{\partial G_i^R(z, z^{'}; E)}{\partial z}/G_i^R(z, z^{'}; E)] \tag{2.15}$$

Since $Z_i(z, z'; E)$ has a discontinuity at $z = z'$ owing to the property of G^R, one needs two boundary conditions to determine $Z_i(z, z'; E)$. To obtain these boundary condi-

tions, we assume that the potential profile is flat sufficiently far from the semiconductor oxide interface in both directions. If $V(\infty)$ is the constant potential at $z = \infty$ (deep inside the semiconductor) and if $V(-\infty)$ is the constant potential at $z = -\infty$ (deep inside the gate metal), Green's function in those regions may be expressed as,

$$G_i^R(z \longrightarrow \infty, z'; E) \sim e^{\gamma_i(\infty)(z-z')} \tag{2.16}$$

and

$$G_i^R(z \longrightarrow -\infty, z'; E) \sim e^{-\gamma_i(-\infty)(z-z')} \tag{2.17}$$

where $\gamma_i(\pm\infty) = i\sqrt{(2m_{zi}/\hbar^2)(E - eV(\pm\infty) + i\epsilon)}$. The boundary conditions to estimate Z_i are determined from Eq. (2.16) and (2.17). These are,

$$Z_i(z \longrightarrow \infty, z'; E) = Z_{oi}(\infty), z > z' \tag{2.18}$$

and

$$Z_i(z \longrightarrow -\infty, z'; E) = Z_{oi}(-\infty), z < z' \tag{2.19}$$

where, $Z_{oi}(\pm\infty) = (2\hbar/im_{zi})\gamma_i(\pm\infty)$. From the properties of 1D Green's functions, it can be shown [12], for all $z > z'$:

$$Z_i(z, z'; E) = Z_i^+(z; E) \tag{2.20}$$

for all $z < z'$,

$$Z_i(z, z'; E) = Z_i^-(z; E) \tag{2.21}$$

here, $Z_i^+(Z_i^-)$ does not depend on z' as long as $z > z'$ $(z < z')$. Using the asymptotic boundary conditions, $Z_i^{\pm}$ are calculated as functions of z using a method analogous to the impedance transformation technique of microwave transmission lines [19].

the normalized wave function can be obtained from retarded Green's function. We have G_i^R expressed as a function of complete set of eigenfunctions,

$$G_i^R(z, z'; E) = \sum_j \frac{\psi_{ij}(z)\psi_{ij}^*(z')}{E - E_{ij} + i\epsilon} \tag{2.22}$$

If $E_{i(j+1)} - E_{ij} >> \epsilon$ for all values of j, only one term dominates when $E \to E_{ij}$, as the discrete eigenenergies are degenerate. For the diagonal elements of G_i^R, we obtain

$$G_i^R(z, z'; E \to E_{ij}) \cong \frac{|\psi_{ij}(z)|^2}{E - E_{ij} + i\epsilon} \tag{2.23}$$

Equating imaginary parts of (2.23) and putting $E = E_{ij}$,

$$|\psi_{ij}(z)|^2 = -\epsilon Im[G_i^R(z, z'; E_{ij})] \tag{2.24}$$

It has been shown in [12] that,

$$-Im[G_i^R(z,z';E_{ij})] = \frac{4}{\hbar} Im(\frac{i}{Z_i^+(E_{ij}) - Z_i^-(z;E_{ij})}) \tag{2.25}$$

From (2.25) in (2.24),

$$|\psi_{ij}(z)|^2 = \frac{4\epsilon}{\hbar} Im(\frac{i}{Z_i^+(z;E_{ij}) - Z_i^-(z;E_{ij})}) \tag{2.26}$$

The 1D state of density N_{1D} is related to the diagonal part of G^R. $N_{1D_i}(z;E)$, in terms of retarded Green's function, G_i^R is given by,

$$N_{1D_i}(z;E) = -\frac{1}{\pi} Im[G_i^R(z,z';E)] \tag{2.27}$$

When $\epsilon \to 0^+$, the density-of-states (DOS), $N_{1D_i}(z;E)$, becomes a delta function at the eigenenrgies, $E = E_{ij}$ in a bound system with the amplitude equal to the probability density at that energy, i.e.,

$$N_{1D_i}(z;E) = \sum_j |\psi_{ij}(z)|^2 \delta(E - E_{ij}) \tag{2.28}$$

In case of inelastic scattering or leaky potential well, G_i^R is defined by (2.14) where ϵ replaced by V_i. Here $V_i = \hbar/2\tau_i$ where τ_i is the phase breaking in case of inelastic scattering and is the carrier lifetime in the quantum well in presence of leaky well. If E approaches E_{ij}, the density of states is given by the familiar Lorentzian shape:

$$N_{1D_i}(z;E) = \frac{V_i}{\pi} \frac{|\psi_{ij}(z)|^2}{(E - E_{ij})^2 + V_i^2} \tag{2.29}$$

Using Eq. (2.27), N_{1D} can be expressed in terms of the logarithmic $Z_i^{\pm}$ [12]:

$$N_{1D_i}(z;E) = \frac{4}{\pi\hbar} Im(\frac{i}{Z^+(z;E) - Z^-(z;E)}) \tag{2.30}$$

The eigenenergies of a quasi bound state E_{ij} can easily be found by locating peaks of N_{1D_i}, evaluated using Eq. (2.30). Once the eigenenergies have been found, the normalized wave function can be calculated using Eq. (2.26).

2.2.4 Incorporating Wave Function Penetration in Self-consistent Model

So far carrier properties in MOS inversion layers are studied by solving coupled schrödinger's and Poisson's equation. Considering effective mass approximation 3D schrödinger's equation is decoupled into a 1D equation that is a envelope function in the direction normal to the interface. For a parabolic bandstructure, 1D schrödinger's equation is given by (2.3). But this does not include wave-function penetration. To incorporate wave-function penetration an open boundary condition is required at the silicon-oxide interface. This should take into account the quasi-bound nature of the inversion layer states.

Open boundary conditions are based on this that the potential profile is flat at deep inside the gate metal as well as at deep inside bulk semiconductor. This assumption states that the wave function deep inside the semiconductor is exponentially decaying ($E < eV(\infty)$) and deep inside the gate metal, the wave function is a plane wave ($E > eV(-\infty)$).

As a fraction of inversion charge resides within the gate oxide due to wave function penetration, Poisson's equation be solved for the combined oxide and semiconductor region. Considering wave-function penetration we have,

$$\frac{d^2V(z)}{dz^2} = \begin{cases} -\frac{\rho_{inv}(z)}{\epsilon_0\epsilon_{ox}}, & -T_{ox} < z < 0 \\ \frac{\rho_{inv}(z)+\rho_{depl}(z)}{\epsilon_0\epsilon_{si}}, & z > 0 \end{cases} \tag{2.31}$$

where,

$$\rho_{inv}(z) = -e\sum_{ij} N_{ij}|\psi_{ij}(z)|^2 \tag{2.32}$$

and $\rho_{inv}(z)$ is defined by Eq. (2.7). In Eq. (2.32), N_{ij} is given by Eq. (2.6). When $|\psi_{ij}(z)|^2$, calculated with penetration is used to define ρ_{inv} in Eq. (2.32), effects of shift of inversion charges on the solution of Poisson's equation are also included.

The boundary conditions required to solve Eq. (2.31) can no longer be applied at the semiconductor-oxide interface due to the presence of inversion charges in the oxide. Here new boundary condition that is used is given by, dV/dz vanishes for large z and that its value at the gate metal-oxide interface ($z = -T_{ox}$) be -F_{ox}, where

$$F_{ox} = e(N_{inv} + N_{depl})/\epsilon_0\epsilon_{ox} \tag{2.33}$$

N_{inv} and N_{depl} can be found from (2.10) and (2.13). it is assumed in (2.33) that wave function tail has decayed to an insignificant value at $z = -T_{ox}$. But this is valid only for devices with $T_{ox} \geq 0.5nm$. Another relationship necessary is relation between F_{ox} and F_s at $z = 0$. It is, $\epsilon_{ox}F_{ox} = \epsilon_{si}F_{si}$.

Under the modified self-consistent analysis Eqs. (2.3) and (2.31)-(2.33) are solved iteratively. The calculation is started with small value of N_{inv} and then gradually increasing its value. In each case result of last iteration is taken to be the starting of the next. Initial potential is found by taking $N_{inv} = 0$. For a given potential $V(z)$, the eigenenegy of the quasi bound state E_{ij} is found by locating the peaks of N_{1D_i} where the 1D DOS,

N_{1D}, is calculated using Eq. (2.30). The logarithmic derivative $Z_i^{\pm}$ can be estimated as functions of z using Eqs. (2.18) and (2.19) [19]. So wave-function penetration included wave-functions can be calculated from (2.26). After this Fermi energy E_F can be found from (2.6) and (2.10) for a given N_{inv}. Once Fermi energy is known, N_{ij} for each sub-band can be found from (2.6). $V(z)$ is found by solving Poisson's equation described in (2.31) and (2.32) with boundary condition (2.33). Now new values of E_F and E_{ij} are found from Schrödinger's equation, which is resolved in the manner just described. Poisson's equation can be solved again and again before it converges.

For convergence purpose percent change in Fermi energy E_F and first eigenstate E_{i1} of the new iteration is compared with that of previous one. The loop is terminated if a accuracy of 0.005% or less is reached. Complete flowchart is given in Appendix A.

2.3 Compact model

As mentioned earlier, Li et al. introduced a computationally efficient compact model to simulate C-V for ultrathin gate dielectrics. Wave function penetration effect is considered. Authors assumed that a small interfacial layer of SiO_2 is present between gate dielectric and Si substrate. They also proposed that this model is valid for pure high-k materials [11].

The triangular-potential approximation of the MOS potential well (the dielectric approximated as an infinite potential barrier and the slope of the potential in Si defined by the surface electric field) leads to Airy function solution for the first eigenenergy as,

$$E_1 \approx \left(\frac{\hbar^2}{2m^*}\right)^{\frac{1}{3}} \left[\frac{3}{2}\pi e F_s \left(1+\frac{3}{4}\right)\right]^{\frac{2}{3}} \tag{2.34}$$

Where m^* is the quantization effective mass, E_1 is ground state eigenenergy and F_s represents the surface dielectric field [4]. Although, Airy function solution provides

compact analytic expression, it is inaccurate due to (i) linear approximation of the potential profile inside Si and (ii) the negligence of wave function penetration into the dielectric layer. Compact model introduced by Li et al. [11] overcomes these limitations by taking the effects of wave function penetration and non-triangular potential profile into account. In [11], the authors proposed that the form of the 2/3 power law for the eigenenergy would be the same, only the value of exponent over oxide field should be refined. They calculated first eigenenergy for electrons and holes as,

$$E_1 - E_{c,v} \cong \pm\gamma \left(\frac{|F_{ox}|\, cm}{MV} \right)^{\lambda} \tag{2.35}$$

Where, E_c is the conduction band edge and E_v is the valence band edge at the Si-dielectric interface, F_{ox} is the effective oxide field and E_1 is the first eigenenergy. λ is the modified exponent of the power law relationship. Li et al. showed that for electrons λ = 0.61 and γ = 77 meV and for holes λ = 0.64 and γ = 88 meV. Ref. [11] showed all the necessary calculations considering SiO_2 as gate dielectric material. [11] did not consider doping density $N_{a,d}$ and characteristics of dielectric material to have any impact on the values of λ and γ. For high-k materials these values may not be reliable.

C-V curves are obtained from the model of Li et al. as follows. In strong inversion or accumulation of the channel, once the eigenenergies have been calculated, the Fermi level is established by the charge occupation of these levels. The total field-induced mobile surface charge density is approximated by,

$$Q_s(F_{ox}) = -\epsilon_{ox} F_{ox} \tag{2.36}$$

in accumulation, and

$$Q_s(F_{ox}) = -\epsilon_{ox} F_{ox} - Q_{depletion}(F_{ox}) \tag{2.37}$$

in strong inversion, where ϵ_{ox} is the dielectric constant of the oxide and $Q_{depletion}$ is the depletion region charge as a function of the oxide field. In strong inversion, the po-

tential energy drop across the depletion region (but not including the strong inversion layer) is approximated as,

$$q\psi_{d,si}(F_{ox}) = \pm 2q\phi_F + [E_1(F_{ox}) - E_{c,v}(F_{ox})] \tag{2.38}$$

where $q\phi_F$ is, as usual, the magnitude of the separation between the Fermi level and the intrinsic Fermi level at flatband. The addition of E_1 approximates the effective increase in magnitude of the band edge due to quantum confinement. The required depletion layer charge in strong inversion required is,

$$\mp Q_{depletion}(F_{ox}) \cong \sqrt{2q|\psi_{d,si}(F_{ox})|\epsilon_s N_{dop}} \tag{2.39}$$

for electrons and holes, respectively, where ϵ_s is the dielectric constant in Si. Applying Fermi Dirac statistics within an effective mass approximation such that there is a constant density of states in each subband,

$$\mp Q_s(F_{ox}) = \sum_i \frac{\eta_i m_i k_B T}{\pi\hbar^2} \ln(1 + \exp\frac{\pm[E_F - E_i(F_{ox})]}{k_B T}) \tag{2.40}$$

for electrons and holes, respectively, (where all energies are given for electrons even for valence band states), η_i is the degeneracy of the ith eigenenergy level, m_i is the two-dimensional interface-parallel density of states effective mass which depends on which valley the ith eigenenergy level is in, and E_F is the Fermi level. Assuming a known occupancy factor for the groundstate subband κ_1,

$$\mp \kappa_1 Q_s(F_{ox}) = \frac{\eta_1 m_1 k_B T}{\pi\hbar^2} \ln(1 + \exp\frac{\pm[E_F - E_1(F_{ox})]}{k_B T}) \tag{2.41}$$

This latter equation can be solved explicitly for $E_F - E_{c,v}(F_{ox})$ in terms of $E_1(F_{ox}) - E_{c,v}(F_{ox})$ and $Q(F_{ox})$,

$$E_F - E_{c,v}(F_{ox}) = E_1(F_{ox}) - E_{c,v}(F_{ox}) \pm \kappa_B T \ln[\exp(\frac{\kappa_1|Q_s(F_{ox})|\pi\hbar^2}{e\eta_1 m_1 \kappa_B T}) - 1] \tag{2.42}$$

for electrons ($\eta_1 = 4$ including spin degeneracy) and holes ($\eta_1 = 2$), respectively, for the compact model. The constant values of κ_1 used in this paper are 0.65 for electrons

in inversion (n-MOS) and 0.57 in accumulation (p-MOS), and 0.86 for holes in inversion (p-MOS) and 0.83 in accumulation (n-MOS). $\pm 10\%$ variation of κ_1 does not have any reasonable effect on C-V curves.

The total band-bending in the substrate, the surface potential, is then given by,

$$q\varphi_{sub}(F_{ox}) = [E_F - E_{c,v}(F_{ox})] - [E_F - E_{c,v}(0)] \tag{2.43}$$

where $E_F - E_{c,v}(0)$ is the relative position of the Fermi-level at the interface at flat-band.

In weak inversion, in the simplest approach, the surface charge layer is neglected along with the associated challenges considered above. In this regime, Li's compact model becomes quite conventional; the total band bending in the substrate is calculated,

$$q\varphi_{sub}(F_{ox}) = \pm\frac{\epsilon_{ox}^2 F_{ox}^2}{2q\epsilon_s N_{dop}} \tag{2.44}$$

for n-MOS and p-MOS, respectively. For metal gates, once the $\varphi_{sub}(F_{ox})$ is known in accumulation, depletion and weak inversion, or strong inversion, the gate voltage, $V_G = -[E_{F,Gate} - E_F]/q$, is given by,

$$V_G = V_{FB} + F_{ox}t_{ox} + q\varphi_{sub}(F_{ox}) \tag{2.45}$$

where t_{ox} is the equivalent oxide thickness, F_{ox} is the effective oxide field, and $q\varphi_{sub}(F_{ox})$ is the total band bending/surface potential in the substrate. Total charge is given by,

$$Q_{tot} = \epsilon_{ox}F_{ox} \tag{2.46}$$

The gate capacitance value is obtained as,

$$C = \frac{\partial Q_{tot}}{\partial V_G} \tag{2.47}$$

In order to calculate C-V characteristic the steps to be followed are: (i) for strong in-

version, to calculate first eigenenergy (E_1) using Eq. (2.35), to calculate Q_s from Eq. (2.38), Eq. (2.39) and Eq. (2.37), and for accumulation, to calculate Q_s from Eq. (2.36), (ii) to calculate $E_F - E_{c,v}(F_{ox})$, (iii) for strong inversion or accumulation, to calculate φ_{sub} from Eq. (2.43), for weak inversion or depletion, to calculate φ_{sub} from (2.44) and (iv) to calculate capacitance form Eq. (2.45), Eq. (2.46) and finally Eq. (2.47). Since, self-consistent calculations are not required for the calculation of C-V, this model is computationally efficient and computation time is very small, and thus this model is a compact model.

2.4 Proposed Compact Model

As mentioned earlier, in the model of Ref. [11], λ was considered to be constant irrespective of the dielectric material and substrate doping density of the device. Hence, the use of the model for MOS devices consisting of different high-k gates and different substrate doping densities is not justified. To resolve this problem, we have assumed λ to be a function of characteristics of dielectric materials and substrate doping density as given by Eq. 1.1. However, compact model is not sensitive to the variation of γ. In order to include these effects on λ, we have performed numerical self-consistent simulations of E_1 for MOS structures with different dielectric materials and different substrate doping densities and for different metal gate. By fitting these data with Eq. 2.35, the dependence of λ on dielectric properties and doping density may be determined to determine the unknown function 1.1.

Once the function of λ is determined, Eqn. 1.1 may be employed to determine the value of λ for a particular MOSFET. With this value of λ the C-V characteristics for the MOSFET may be simulated easily and accurately by using the calculations shown in previous section.

Since, this simulator uses Green's function formalism and considers wave-function penetration into the gate dielectric material [9], accurate modeling of gate capacitance is possible via this compact model.

2.5 Other Theories Used

In order to evaluate correct C-V curve for a specific device from our improved compact model, it is necessary to extract effective oxide thickness EOT, doping density $N_{a,d}$ and flat-band voltage V_{fb} from experimental C-V curves accurately. For this we have used two unique theories.

2.5.1 Extraction of EOT

Compact model is very sensitive to EOT. Only two parameters that vary in compact model of Li et al. [11] are EOT and doping density. Slight change in EOT can make significant variation in C-V curve slope. As our improved compact model is similar to the model of [11] in all aspects except λ, EOT is also vital here. So accurate measurement of EOT is very essential to reproduce compact model [11] as well as our improved compact model.

A lot of methods are proposed to calculate EOT from C-V characteristics. A method is proposed in [20] and [21]. But it fails to evaluate EOT with ultrathin gate dielectric. It is inaccurate even for SiO_2. It is common to find T_{di} and C_{di} by matching simulated C-V with measured data as shown in [22] and [23]. EOT is calculated from C_{di}. But this method is prone to error due to lack of self consistency, consideration of small number eigenstates and avoidance of wave function penetration. Kar has proposed a method to find EOT and some other parameter's value in [20] and [21]. But it is assumed that C_{acc} (accumulation capacitance) is exponentially dependent on ϕ_s (surface potential). For this accuracy of this method cannot be verified. Ahmad et al showed a quantum mechanical approach to extract EOT with ultrathin gate dielectrics considering wave function penetration. This model is based on self-consistent solution of one-dimensional Schrödinger and Poisson's equation. We have used this model to extract EOT.

Mathematical approach used in Ahmad's model is given below. 1-D Schrödingers equation is solved using a technique based on the Greens function formalism with transmission line analogy. The carrier density in bound states N_{ij}, associated with the

jth subband in the ith valley, is calculated using the procedure of Haque et al. [9]. This model is capable of considering any value or energy (or bias) dependent function for carrier effective mass within the dielectric region m_{di}. The total charge density at any position z (normal to the Si-dielectric interface) in p-MOS is expressed as,

$$p(z) = N_D^+(z) - eN_{acc}$$

and

$$N_{acc} = \sum_i \sum_j N_{ij}|\psi(z)|^2 + N_{cl}(z)$$

where $N + D(z)$ is the distribution of ionized donors, $N_D^+(z)$ is the electron wave function, and $N_{cl}(z)$ is the semiclassical distribution of carriers in the extended states. p(z) is used to solve the Poissons equation in the combined oxide semiconductor regions. Once the self-consistent loop converges, C_{acc} and C_g are calculated from the basic definitions $C_{acc} = e\partial N_{acc}/\partial\phi_s$ and $C_g = e\partial N_{acc}/\partial V_g$.

It was assumed that C_{acc} is exponentially dependent on ϕ_s in Kar's method. This does not give accurate results in all cases. Ahmad et al. in [7] has shown this dependence in three different regions. C_{acc} varies exponentially in weak accumulation, linearly in moderate accumulation and sub-linearly in strong accumulation with ϕs. Weak accumulation region is not important to calculate C_{di} rather than moderate and strong accumulation regions. Only drawback of this algorithm is it can work only if interface trap charge is low or C_{it} is under certain limit.

C_{acc} versus ϕ_s in all three regions can be accurately fitted by a curve that is Boltzmann-type curve. Region 2 and 3 are of main importance. So they should be modeled with accuracy. Typical equation that is given to represent them are as follows:

$$C_{acc} = a_1 - a_2 exp(-a_3\phi_s) - a_4 exp(-a_5\phi_s)$$

But this equation has too many parameters. So accurate modeling of C_{di} is complicated. Remedy of this problem is to find a equation for linear region 2. Thus for both n-MOS

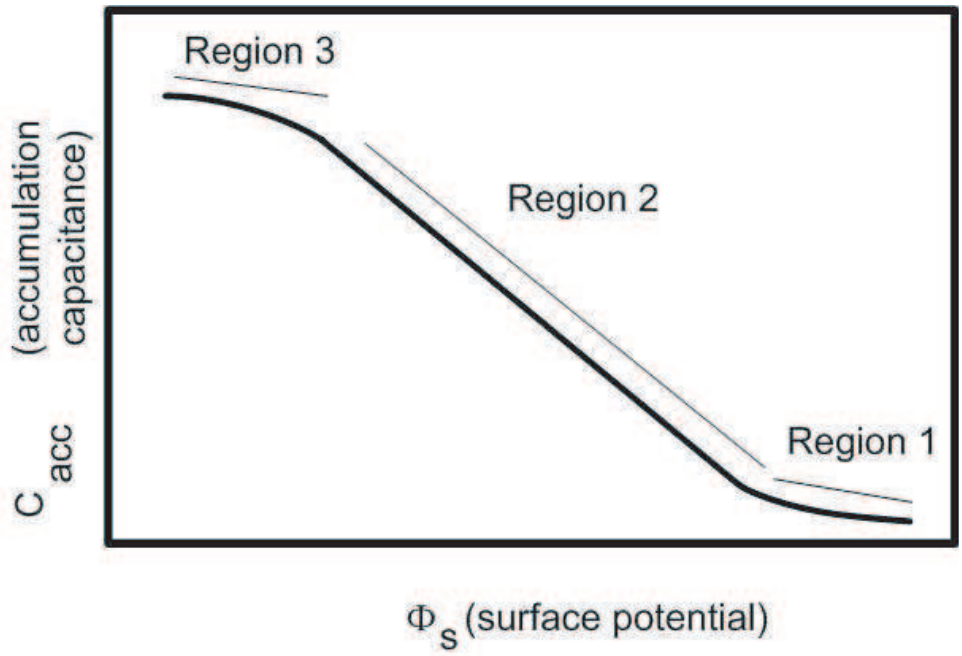

Figure 2.7: Different regions of C_{acc} vs. ϕ_s curve.

and p-MOS devices we can write,

$$C_{acc} = a_{acc} + b_{acc}\phi_s$$

The total parallel capacitance $C_p = C_{acc} + C_{it}$ in moderate and strong accumulation is then nearly equal to C_{acc}. Differentiating C_p with respect to V_g we have,

$$\frac{d\phi_s}{dV_g} = 1 - \frac{C_g}{C_{di}}$$

and,

$$\frac{dC_p}{dV_g} = b_{acc}(1 - \frac{C_g}{C_{di}})$$

Noting that C_g is equal to the series combination of C_{di} and C_p, differentiating C_g with respect to V_g to obtain,

$$(\frac{dC_g}{dV_g})^{\frac{1}{3}} = b_{acc}^{\frac{1}{3}}(\frac{C_g}{C_{di}})$$

From this a plot of $|\frac{dc_g}{dV_g}|^{1/3}$ vs. C_g is performed. Most of this plot is linear. A linear line

is fitted through this curve. The line intersects C_g axis in C_{di} value. From C_{di} we can get EOT by following formulae,

$$C_{di} = \frac{\epsilon_0 \epsilon_{di}}{T_{ox}}$$

$$EOT = \frac{T_{ox} \times 3.9}{k_{di}}$$

Here, T_{ox} = Oxide thickness, k_{di} = Dielectric constant. We shall use this technique to evaluate EOT in all cases. In some papers EOT values are given. Using that EOT simulated C-V does not match with the experimental one. This is due to poor instrumental measurement of oxide thickness. But method described by Ahmad et al [7] shows accurate EOT value. Compact model is sensitive to EOT value. Slight change in it can lead to a significant error. Simulation with EOT extracted from the method of Ahmad et al. shows good result than normal EOT value described in data.

2.5.2 Determination of Flat-band Voltage

Flat-band voltage V_{fb} is needed to calculate V_g. V_{fb} has to be determined accurately to place simulated C-V. Otherwise simulated C-V may be placed away from experimental C-V. A lot of methods have been suggested over the past decades to calculate V_{fb}. Haung [24] showed a method to calculate V_{fb} in low temperature. It can be simplified for room temperature but it fails to give correct result in case of high interface charge density. C.C. Cheng [25] found distribution of flat-band volatge in laterally non-uniform MIS capacitor. But calculations given is complicated and V_{fb} is calculated from a function plot that can lead to error. J.S.T. Huang [26] provided V_{fb} dependence on channel length. C.H. Chen calculated EOT by finding flat-band voltage. But there is no clear indication whether this V_{fb} calculation considers interface trap charges or not.

Method that is adopted here to calculate V_{fb} is taken from [27]. In the first step minimum capacitance value is determined from C-V curve. This is taken as the transition point from depletion to inversion. This value is series combination of two capacitance, C_{dmin} (minimum dielectric capacitance) and C_i (insulator capacitance). C_i is deter-

mined from EOT value. From C_{dmin} maximum depletion width is determined as,

$$W_m = \epsilon_0 \epsilon_d / C_{dmin}$$

From W_m, doping density is calculated as,

$$W_m = 2[\frac{\epsilon_s kT \ln(N_a/n_i)}{q^2 N_a}]^{1/2}$$

Here,

N_a = Doping density

ϵ_s = Permitivitty of silicon

After this C_{fb} (flat-band capacitance) is calculated by following formulae.

$$C_{fb} = \frac{C_{ox}\epsilon_s A/(1 \times 10^{-4})(db)}{(1 \times 10^{-12})C_{ox} + \epsilon_s A/(1 \times 10^{-4})(db)}$$

Where, C_{fb} = Flat-band capacitance (pF)

C_{ox} = Oxide capacitance (pF)

ϵ_s = Permittivity of substrate material (F/cm)

A = gate area (cm^2)

1×10^{-4} = Units conversion for db

1×10^{-12} = Units conversion for C_{ox}

And db = Extrinsic Debye length

$$db = (1 \times 10^{-4})[\frac{\epsilon_s kT}{q^2 N_x}]^{1/2}$$

Where, kT = Thermal energy at room temperature (4.046 $\times 10^{21}$ J)

q = Electron charge (1.60219 $\times 10^{-19}$ coul.)

$N_x = N$ at 90% W_m, or N_a, or N_d when input by theuser.

From the value of the C_{fb}, flat-band voltage is calculated. This V_{fb} shows good result with experimental C-V curves. A semiclassical assumption is made here. Lowest

point of C-V characteristics may not be the transition point from depletion to inversion. But error introduced here is not much, and taking this assumption may cause doping density to be varied slightly. Our simulation is not effected considerably by this.

2.6 Parameter Values Used to Develop Improved Compact Model

Dielectric constant and barrier height ϕ_b are two most vital parameters for compact model. Any small deviation from original value of these two can cause significant amount of error in C-V characteristics. So it is necessary to take correct values. Effective mass for holes and electrons are also important parameters for self consistent simulation.

2.6.1 Dielectric Constants

Dielectric constant for different high-k dielectrics are listed below. They are collected from [28].

Material	Dielectric constant
SiO_2	3.9
Si_3N_4	7.0
HfO_2	25
YOSi	14.2
Y_2O_3	15
ZrO_2	25
Al_2O_3	9.0
TiO_2	80

Table 2.1: Different dielectric constant values for dielectric materials

several values of dielectric constants are used for same material. But in our improved compact model and in Li's compact model [11] these values are used.

2.6.2 Barrier Heights

Two barrier height ϕ_b values are used for one dielectric material. One for electron and one for hole. For electrons ϕ_b values are,

Material	ϕ_b (eV)
SiO_2	3.2
Si_3N_4	2.0
HfO_2	1.5
YOSi	3.6
Y_2O_3	2.3
ZrO_2	1.4
Al_2O_3	2.8
TiO_2	1.2

Table 2.2: Barrier height of different dielectric materials for electrons

For holes these values are,

Material	ϕ_b (eV)
SiO_2	4.6
Si_3N_4	2.0
HfO_2	3.1
YOSi	4.5
Y_2O_3	2.2
ZrO_2	5.3
Al_2O_3	4.8
TiO_2	1.2

Table 2.3: Barrier height of different dielectric materials for holes

These values can only be used if a high-k material exists adjacent to Si substrate.

2.6.3 Effective Masses

In all the cases Si substrate is considered to have geometry identical to (111) structure. Negligible error occurs if (111) structure is considered in case of others.

Case	Effective mass, m_0
Holes	$0.25m_e$
Electrons	$0.53m_e$

Table 2.4: Values of effective masses

Here, m_e is the mass of electron = 9.1 $\times 10^{-31}$ kg.

Chapter 3

Simulations and Results

Main drawback of previously published compact model [11] is its independence of λ and γ with doping concentration $N_{a,d}$ and characteristics of dielectric material (ϕ_b, $N_{a,d}$, k and m^*) and characteristic of gate metal (ϕ_m). Without considering these effects, accurate C-V characteristics cannot be generated. It is seen that variation of γ with $N_{a,d}$ or ϕ_b does not have considerable impact on C-V curves. But variation in λ leads to reasonable change in C-V curve's slope. However, from our simulations it is observed that the variation of λ with k, m^* and ϕ_m is insignificant. Thus the Eqn. 1.1 reduced to,

$$\lambda = f(\phi_b, N_{a,d}) \tag{3.1}$$

In this chapter, the method of extracting λ from simulation results will be presented first. It will be followed by the graphical representation of dependence of λ with $N_{a,d}$ and ϕ_b for both electrons (n-MOS inversion and p-MOS accumulation) and holes (p-MOS inversion and n-MOS accumulation). And then the unknown function 3.1 will also be presented. Finally, the validation of our model will be justified by verifying the simulation result with published experimental data.

3.1 Determination of λ

To evaluate λ, a self-consistent simulator is used [9] to calculate the first eigenenergy. To extract λ, E_1 vs. F_{ox} curve is drawn. Both axes are taken to be logarithmic. This will show a line which is about straight. A best fit line is drawn through them as shown in Fig. 3.1-3.4. Slope of this line is required λ. The method is repeated for different substrate doping concentrations ($N_{a,d}$) and different dielectric materials (ϕ_b).

The equation obtained from the best fitting is,

$$y = a + bx \tag{3.2}$$

where, $a = \gamma$, $b = \lambda$, $x = \log(F_{ox})$ and $y = \log(E_1)$

3.1.1 Observations on Values of λ

We took six dielectric materials for this purpose. These are Si_3N_4, HfO_2, ZrO_2, TiO_2, Y-O-Si and Ta_2O_5. Plots of eigenenergy vs. oxide field is shown in Fig. 3.1 and Fig. 3.2 for holes. In Fig. 3.3 and Fig. 3.4 eigenenergy vs. oxide field for electrons is shown with Si_3N_4 and Al_2O_3 as gate dielectric material. Here change in λ for three different doping densities is also seen. Clearly λ does not show a constant value as in [11].

Li et al. [11] proposed λ to be 0.61 for electrons and 0.64 for holes. But their model is accurate for only SiO_2 and SiO_2 gate stack materials. Pure high-k dielectrics have no interfacial layer and hence barrier height in these conditions cannot be taken to be equal to that of SiO_2. More the deviation of the value of barrier height ϕ_b from SiO_2 value, more is the chance of error in C-V characteristics. Li et al. also proposed λ to be independent of doping density $N_{a,d}$. But our self-consistent simulator shows significant variations in λ with $N_{a,d}$. It is evident that C-V curves will show variations in the shape with the change of $N_{a,d}$. So this variation has to be taken into account for accurate simulation of C-V curves.

Variation of λ suggests that as we change dielectric materials, dependence of first eigenenergy E_1 on oxide field F_{ox} changes. This is due to fact that for different di-

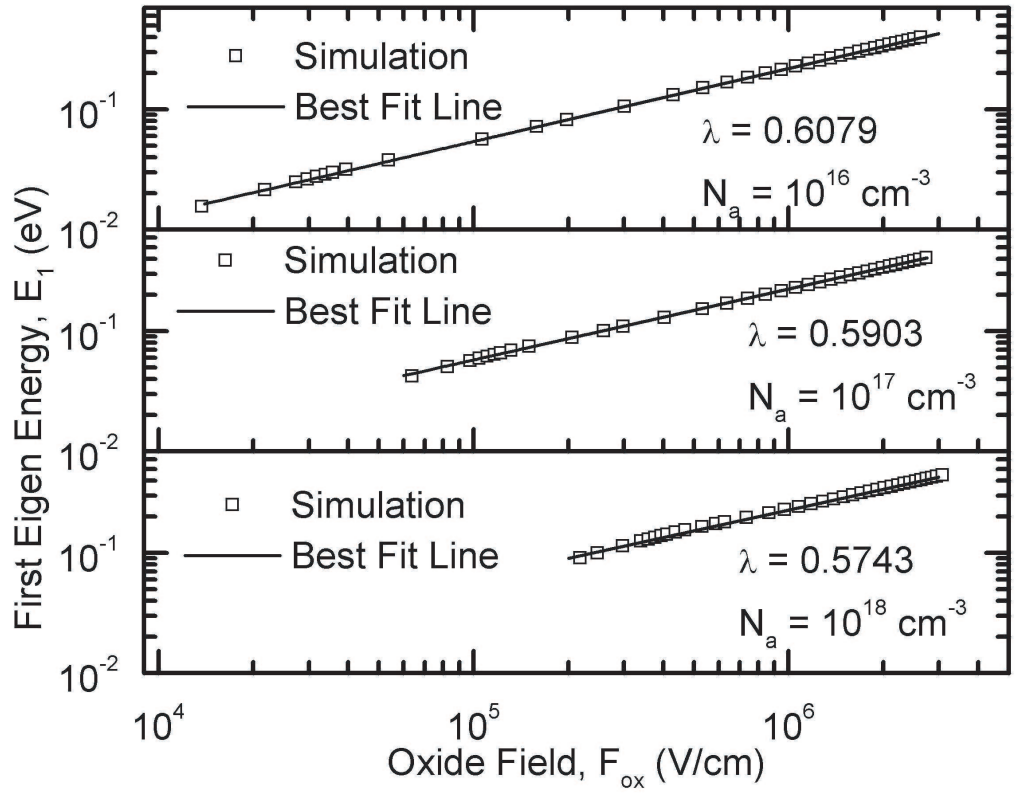

Figure 3.1: E_1 vs. F_{ox} for holes. Gate dielectric used is Y-O-Si for three different doping densities, $10^{16}, 10^{17}$ and 10^{18} cm^{-3}.

electric materials, the barrier height (ϕ_b) is also different.

When $N_{a,d}$ is varied, the triangular well becomes steeper or narrower. So it is expected that E_1 would be different for change in $N_{a,d}$. These changes are not incorporated in model of Li et al. [11]. It will be shown later that these factors are essential for accurate modeling of high-k dielectric C-V characteristics.

3.2 Graphical Representation of λ with ϕ_b and $N_{a,d}$

In this section dependence of λ with ϕ_b and $N_{a,d}$ is shown graphically. In Fig. 3.5 and 3.6 λ is shown as a function of ϕ_b and $N_{a,d}$ respectively for holes. In Fig. 3.7 and 3.8 variation of λ for electrons is given.

As shown in the figures λ increases with increasing barrier height ϕ_b of dielectric ma-

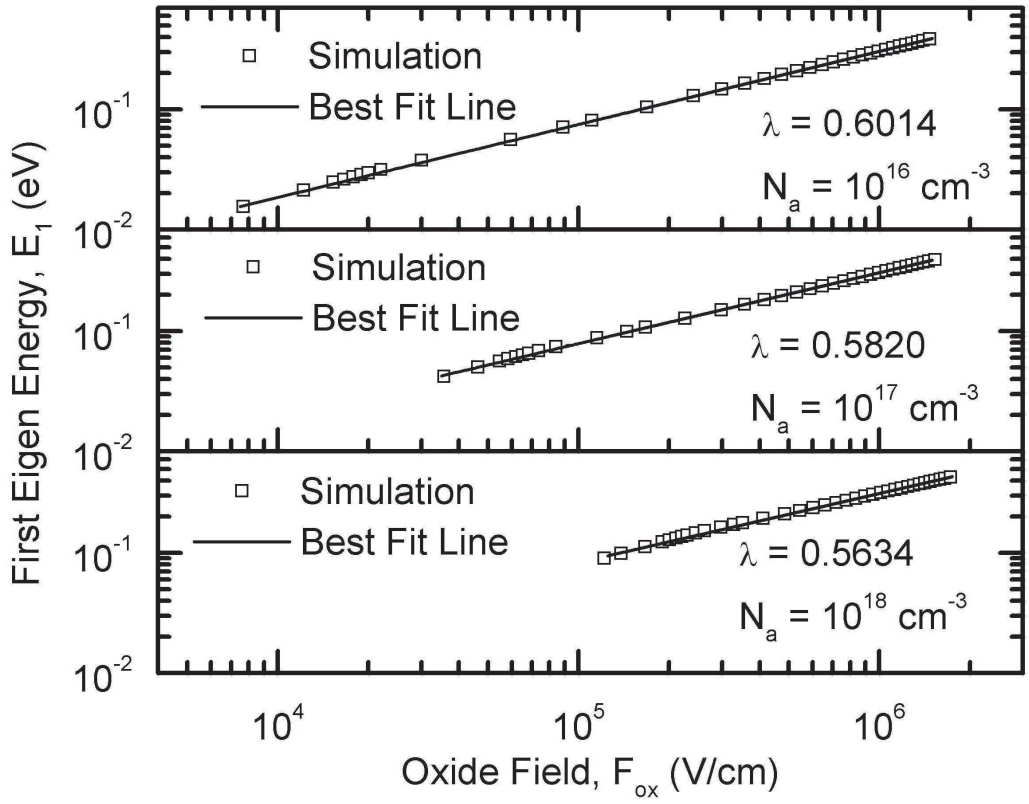

Figure 3.2: E_1 vs. F_{ox} for holes. Gate dielectric used is HfO_2 for three different doping densities, $10^{16}, 10^{17}$ and 10^{18} cm^{-3}.

terials. But it decreases with the increase in doping density $N_{a,d}$. This phenomenon is seen for both electrons and holes. Physical explanation is given below.

3.2.1 Physical Explanation of λ Variation

λ vs. ϕ_b curve follows a typical exponential rising characteristics. More value of λ means first eigenenergy E_1 is more dependent on oxide field F_{ox}. As ϕ_b increases, left margin of potential well in MOSFET also increases. This makes eigenenergies to be spaced with more difference from each other. As γ is constant, λ is the only value to support it. Only increasing λ can prove this theory. On the other hand λ decreases with $N_{a,d}$ increase. A higher doping concentration is responsible for steeper nature of wells. Higher $N_{a,d}$ means lower width of potential well. Eigenenrgies is placed with less differences in a steeper well. Lower value of λ can prove this point. For this reason

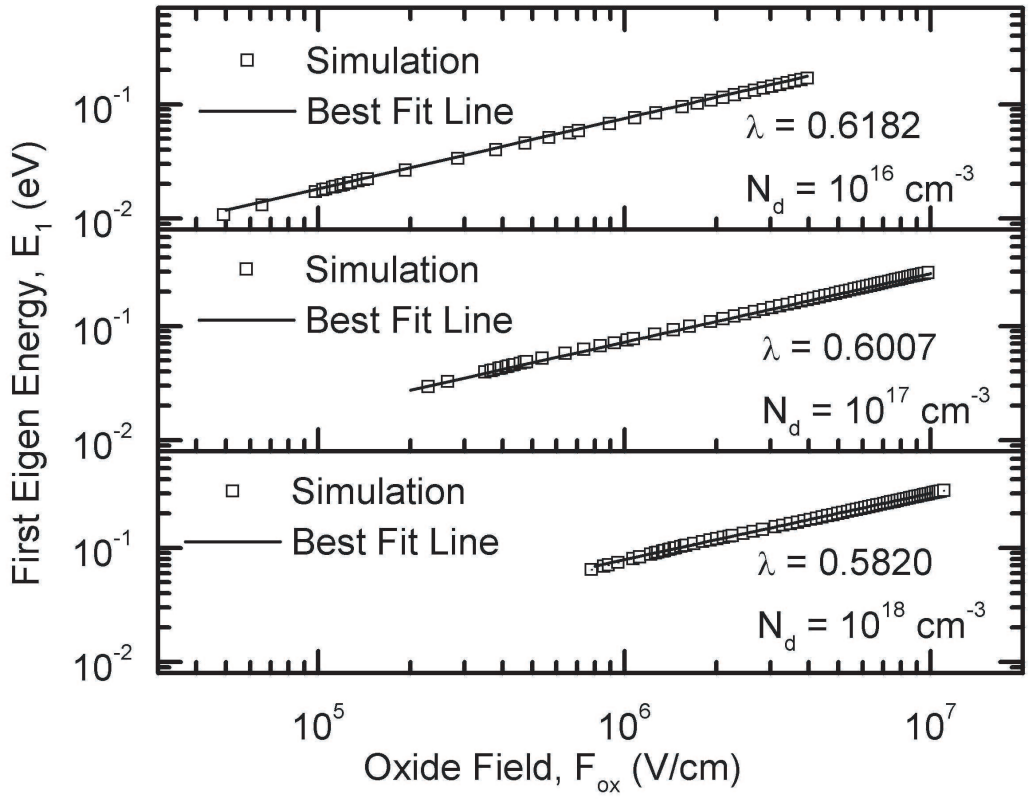

Figure 3.3: E_1 vs. F_{ox} for electrons. Gate dielectric used is Si_3N_4 for three different doping densities, $10^{16}, 10^{17}$ and 10^{18} cm^{-3}.

λ decreases with increasing $N_{a,d}$.

3.3 Empirical Function for λ

It is complex to determine λ from the above plots for different ϕ_b and $N_{a,d}$. Again here only a few values of ϕ_b and $N_{a,d}$ are shown. For any intermediate value, we need interpolation technique. But this is not users friendly. For this reason two equations are formed to calculate λ for holes and electrons. Curve fitting technique is used for equation extraction. As λ is a function of both ϕ_b and $N_{a,d}$, two dimensional equation is given. Though this equation seems a little cumbersome, but it is the best to determine all the values of λ for any values of ϕ_b and $N_{a,d}$ accurately.

Empirical equation that represents function 3.1 to determine λ for holes (p-MOS inver-

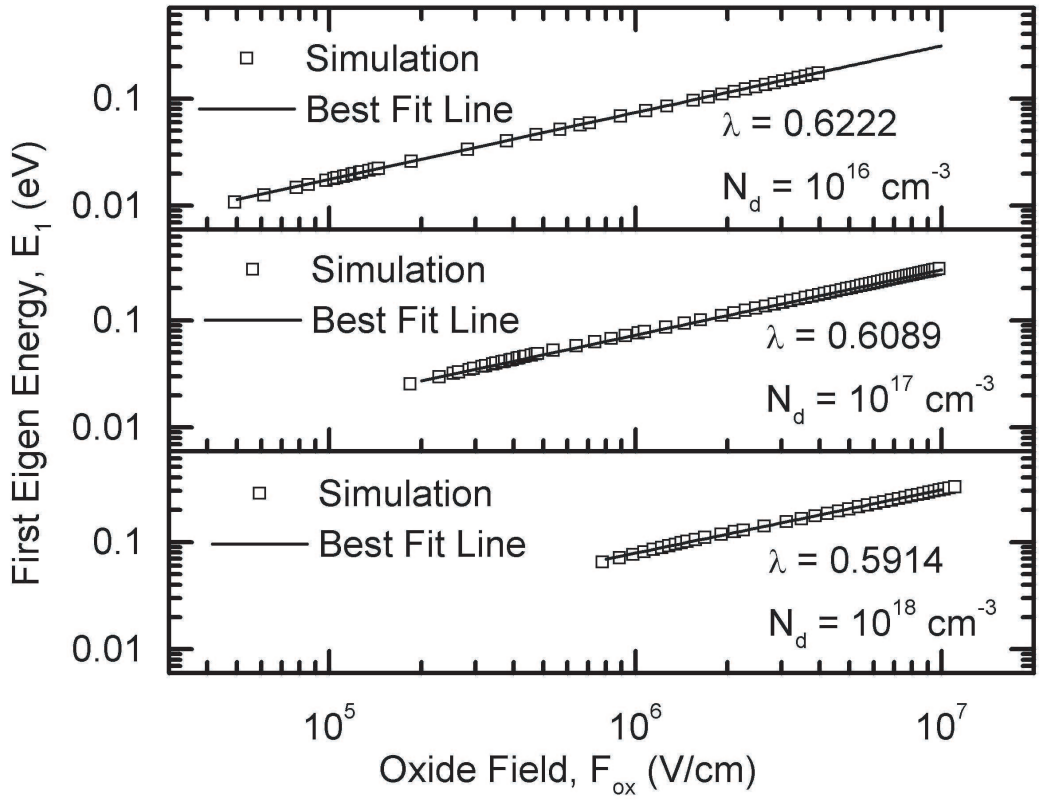

Figure 3.4: E_1 vs. F_{ox} for electrons. Gate dielectric used is Al_2O_3 for three different doping densities, $10^{16}, 10^{17}$ and 10^{18} cm^{-3}.

sion, n-MOS accumulation) is given below.

$$\lambda = \frac{P_1 \times \phi_b + P_2}{\phi_b + P_3} \tag{3.3}$$

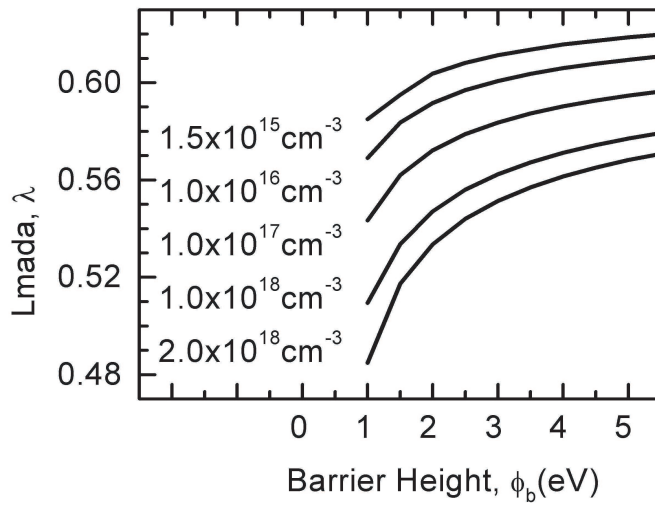

Figure 3.5: λ vs. ϕ_b for different doping densities for holes.

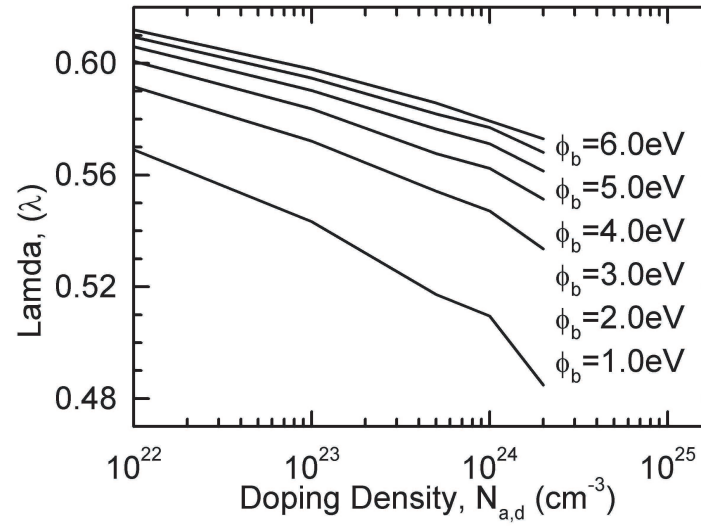

Figure 3.6: λ vs. $N_{a,d}$ for different barrier heights for holes.

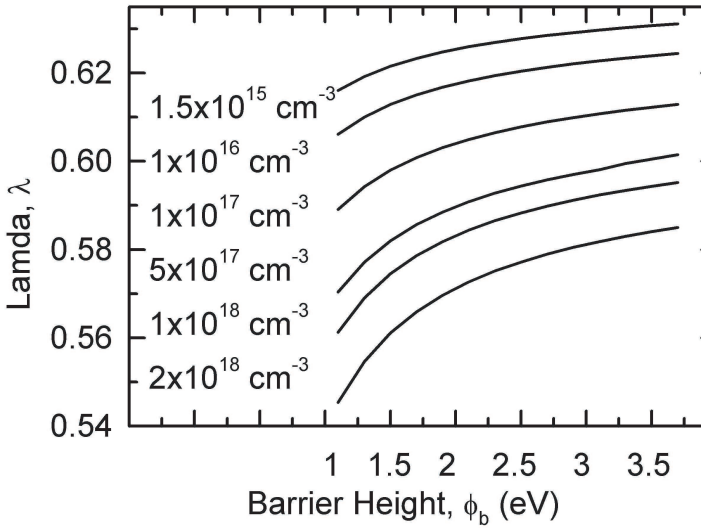

Figure 3.7: λ vs. ϕ_b for different doping densities for electrons.

where, impurity concentration, $N_{imp} = \frac{N_{a,d}(cm^{-3})}{10^{17}}$

And,

$$P_1 = -8.1362 \times 10^{-5} N_{imp}^5 + 0.00294612 N_{imp}^4 - 0.031948 N_{imp}^3 + 0.11673 N_{imp}^2 - 0.108347 N_{imp} + 0.06338 \quad (3.4)$$

$$P_2 = -0.0010917 N_{imp}^5 + 0.03941614 N_{imp}^4 - 0.524591 N_{imp}^3 + 1.52233917 N_{imp}^2 - 1.283078 N_{imp} + 0.3197 \quad (3.5)$$

$$P_3 = -0.001635424 N_{imp}^5 + 0.059014 N_{imp}^4 - 0.63485 N_{imp}^3 + 2.2672 N_{imp}^2 - 1.867476 N_{imp} + 0.06223 \quad (3.6)$$

Equation to calculate λ for electrons (n-MOS inversion, p-MOS accumulation) is given below.

$$\lambda = \frac{P_1 \times \phi_b + P_2}{\phi_b + P_3} \quad (3.7)$$

where, impurity concentration, $N_{imp} = \frac{N_{a,d}(cm^{-3})}{10^{17}}$

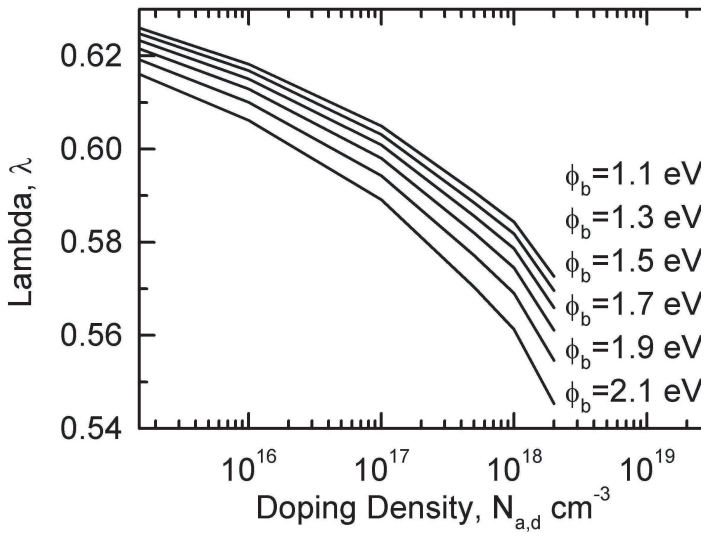

Figure 3.8: λ vs. $N_{a,d}$ for different barrier heights for electrons.

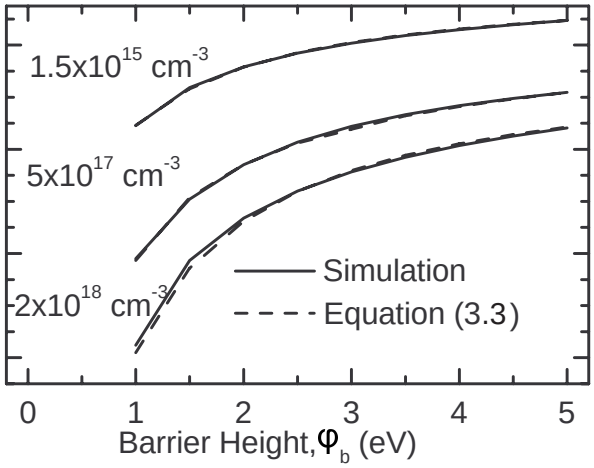

Figure 3.9: Variation of λ with ϕ_b for holes for different doping densities ($N_{a,d}$). Both original simulated curves and equation fitted curves are given.

And,

$$P_1 = -5.005 \times 10^{-5} N_{imp}^5 + 0.0018148 N_{imp}^4 - 0.0197407 N_{imp}^3 + 0.072722 N_{imp}^2 - 0.07048 N_{imp} + 0.6391 \quad (3.8)$$

$$P_2 = -9.755 \times 10^{-5} N_{imp}^5 + 0.00358048 N_{imp}^4 - 0.039882 N_{imp}^3 + 0.15386 N_{imp}^2 - 0.1683 N_{imp} + 0.04982 \quad (3.9)$$

$$P_3 = -6.1225 \times 10^{-5} N_{imp}^5 + 0.00230055 N_{imp}^4 - 0.02676054 N_{imp}^3 + 0.11142 N_{imp}^2 - 0.1431 N_{imp} + 0.1184 \quad (3.10)$$

λ can be calculated from the above equations for any dielectric material and doping density. We have varified our equation approach by plotting curves from the equation over the original curve. This is shown in Fig. (3.9). This shows the accuracy of our proposed method.

3.4 Validity of Improved Compact Model

We have verified our proposed compact model by comparing Capacitance-Gate voltage characteristics obtained from our model with the one from both experiment and

compact model introduced by Li et al [11]. Our model shows less error in all the cases. This makes our model more valid for high-k dielectrics.

3.4.1 Comparison of C-V Characteristics for Holes

We took four experimental C-V curves for comparison for holes (p-MOS inversion and n-MOS accumulation). In each case two more C-V curves are generated with compact model by Li et al [11] and our improved compact model. All three curves are placed in same co-ordinate. For Li et al.'s model C-V $\lambda = 0.64$ for holes is used. Our model's λ value is determined from equation (3.3).

Fig. 3.10 shows experimental and simulated C-V for MOSFET having Y-O-Si as the dielectric material [29]. We have used $N_a = 1 \times 10^{17}$ cm^{-3}, EOT = 1.15 nm and $\phi_b = 4.5$ eV. Here V_{FB} = -0.74 V. V_{FB} and N_a are calculated from the experimental C-V curve. λ from Eqn. (3.3) is 0.595. (3.11) shows error for Li's model and our model. Clearly our model is more accurate at normal operating gate voltage. Maximum error from model of [11] is 3.2% and from our model is 1.1%.

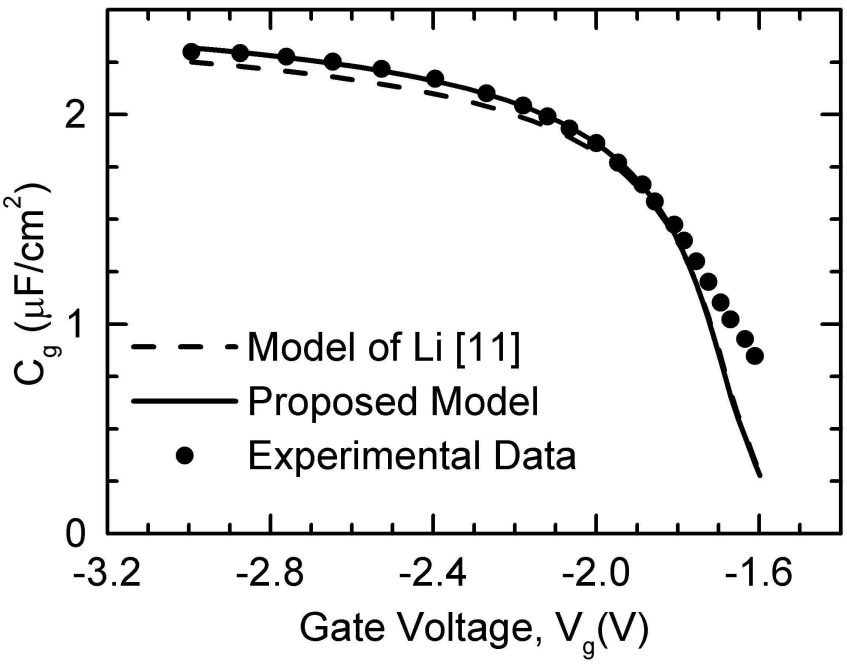

Figure 3.10: C-V curves for YOSi as gate dielectric material. Here doping density $N_a = 1 \times 10^{17}$ cm^{-3}, EOT = 1.15 nm.

Fig. 3.12 shows experimental and simulated C-V for ZrO_2 dielectric material [30]. Data used here are $N_a = 2.1 \times 10^{15}$ cm^{-3}, EOT = 1.1 nm and $\phi_b = 2.0$ eV. Here V_{FB} = -0.38 V. V_{FB} and N_a are calculated with the help of the algorithm stated in theory section. λ from Eqn. 3.3 is 0.60. Fig. 3.13 shows error for model of Li et al. and our model. Here also our model shows less error than the model of [11]. Maximum error from Li's model is 3% and of our model is 1%.

Another C-V comparison is made in Fig. 3.14. Here nitrided ZrO_2 is used as gate dielectric material [30]. Data used here are $N_a = 2.1 \times 10^{15}$ cm^{-3}, EOT = 0.87 nm and ϕ_b = 1.8 eV. Though general barrier height of ZrO_2 is 2.0 eV, here 1.8 eV is used to make compromise with nitride layer in the high-k ZrO_2. This value of ϕ_b is taken from the findings of Ahmad et al [7]. Here V_{FB} = -0.80 V. V_{FB} and N_a are calculated in the same way as before. λ from Eqn. 3.3 is 0.60. Fig. 3.15 shows error for model of Li et al. and our model. Our model shows less error than Li et al.'s model. Maximum error of model of [11] is 5.1% and of our model is 2.1%.

Final C-V comparison is given in Fig. 3.16. Here Si_3N_4 is used as gate dielectric material [31]. Value of parameters are $N_a = 3.7 \times 10^{17}$ cm^{-3}, EOT = 1.56 nm and $\phi_b = 2.0$

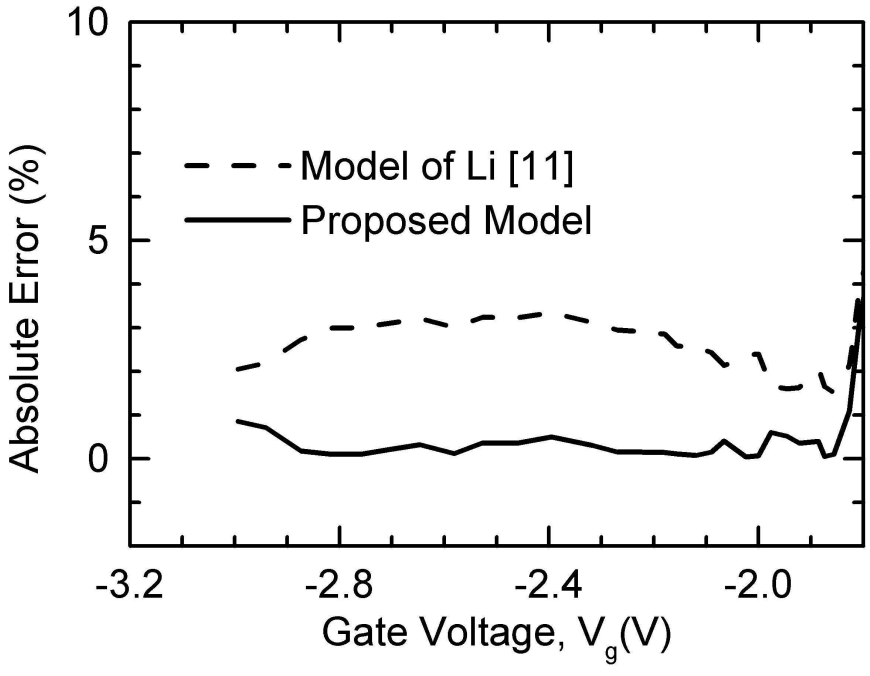

Figure 3.11: Error curve for YOSi as gate dielectric material.

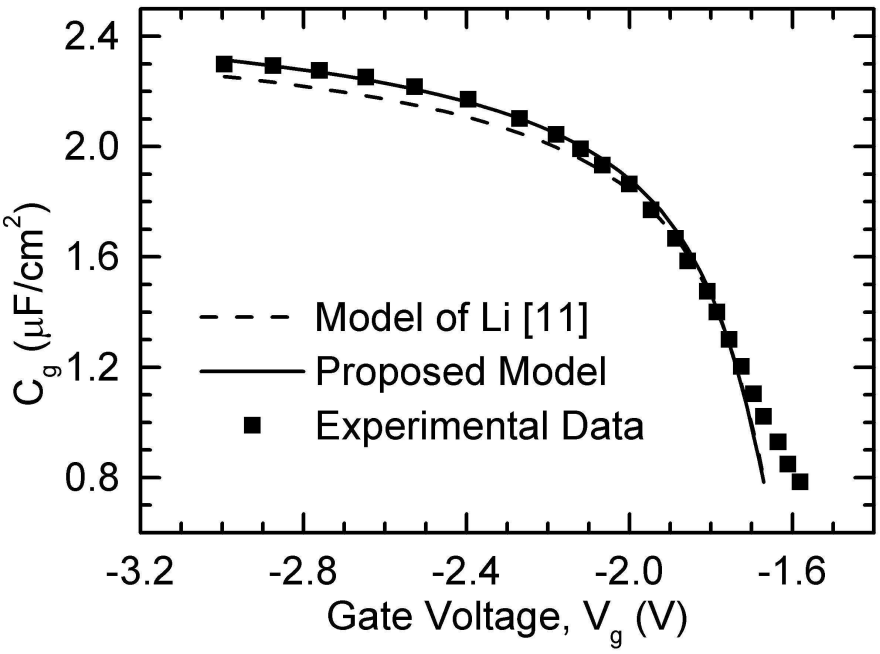

Figure 3.12: C-V curves for ZrO_2 as gate dielectric material. Here doping density $N_a = 2.1 \times 10^{15}$ cm^{-3}, EOT = 1.1 nm.

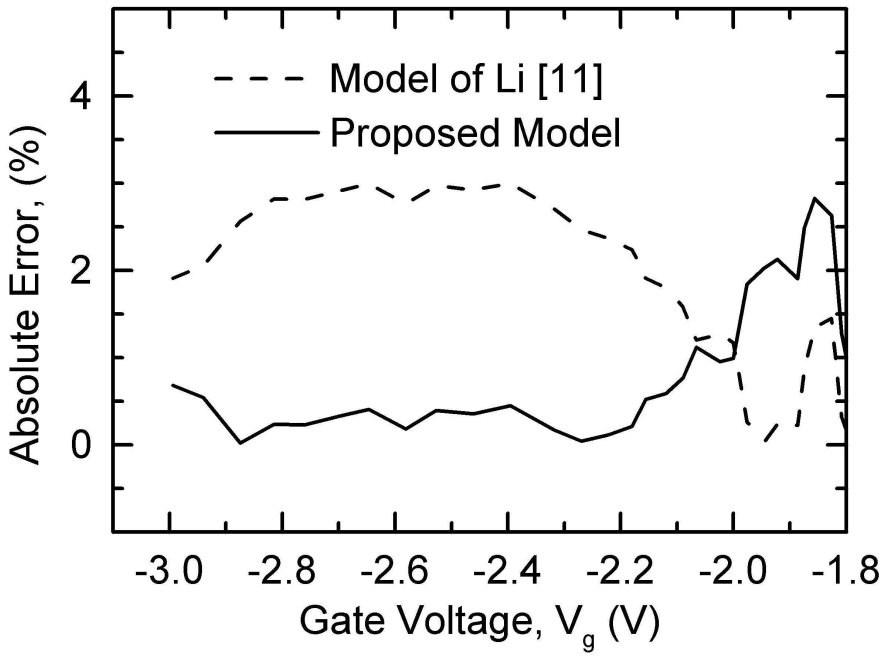

Figure 3.13: Error curve for ZrO_2 as gate dielectric material.

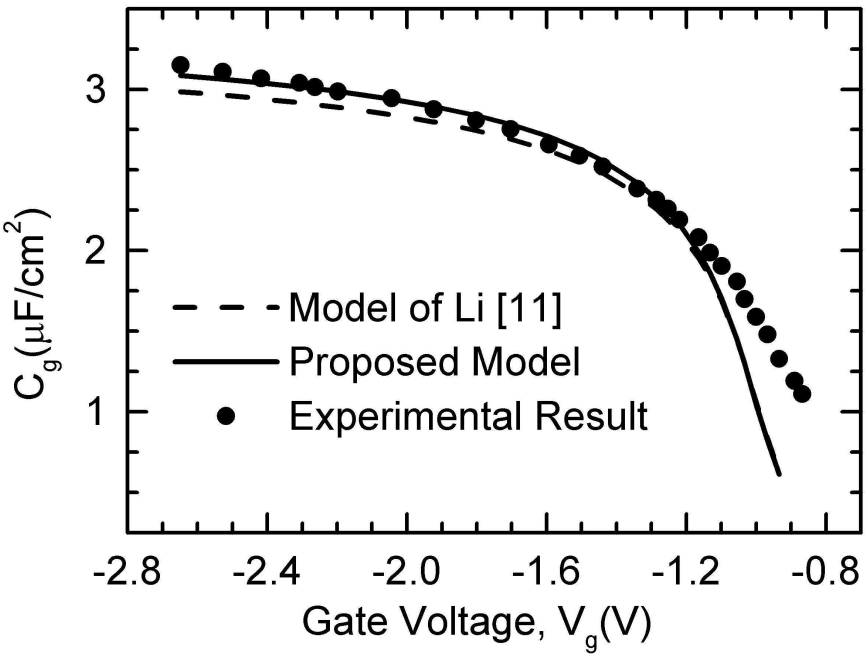

Figure 3.14: C-V curves for nitrided ZrO_2 as gate dielectric material. Here doping density $N_a = 2.1 \times 10^{15}$ cm^{-3}, EOT = 0.87 nm.

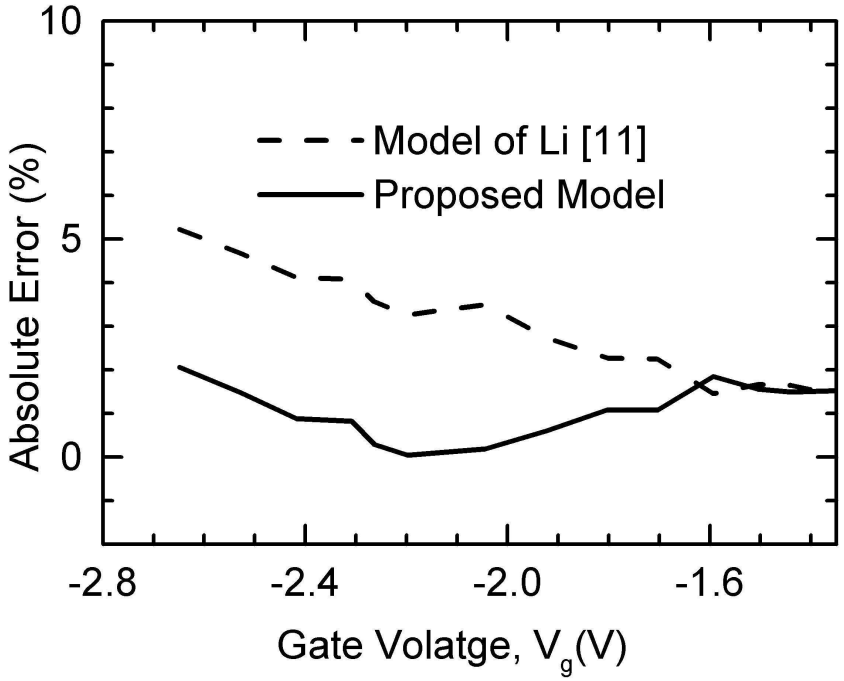

Figure 3.15: Error curve for nitrided ZrO_2 as gate dielectric material.

eV. λ from Eqn. 3.3 is 0.5875. Fig. 3.17 shows error both models. Once again our model shows less error. Maximum error from Li's model is 2.5% and from our model is 1.3%.

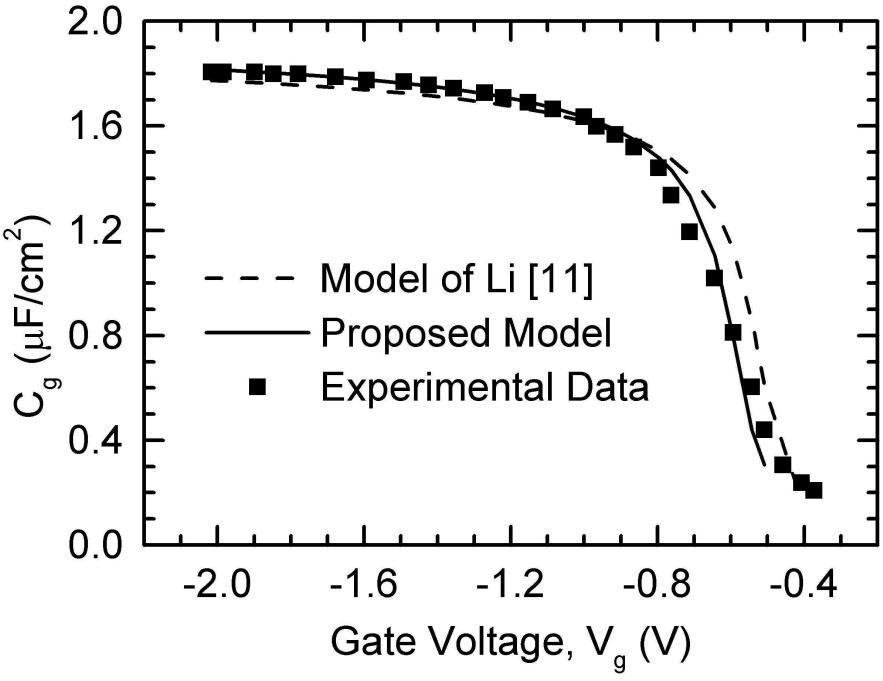

Figure 3.16: C-V curves for Si_3N_4 as gate dielectric material. Here doping density $N_a = 3.7 \times 10^{17}$ cm^{-3}, EOT = 1.56 nm.

Maximum error in our proposed model in these examples is 1.3%. In most of the gate voltage region error is near 0%. This proves the validity of improved compact model. Constant λ value keeps the slope of C-V characteristics inadequate to real result. Variation in ϕ_b and $N_{a,d}$ have to be considered for accurate modeling of C-V curves. In accumulation region our curve is not well matched. This is because in weak accumulation region capacitance C_g is exponentially dependent on surface potential ϕ_s. Compact model by Li et al. cannot model C-V in this region via general procedure. As we took full algorithm of Li et al. as improved compact model except value of λ, it is customary that we cannot match C-V in weak accumulation region. But our result is better in strong accumulation region. Li et al. neglects the slope of C-V in this region. For inversion region our model is better as well agreed with experimental data in all regions. Here our proposed improved compact model outperforms the model of Li et al. [11].

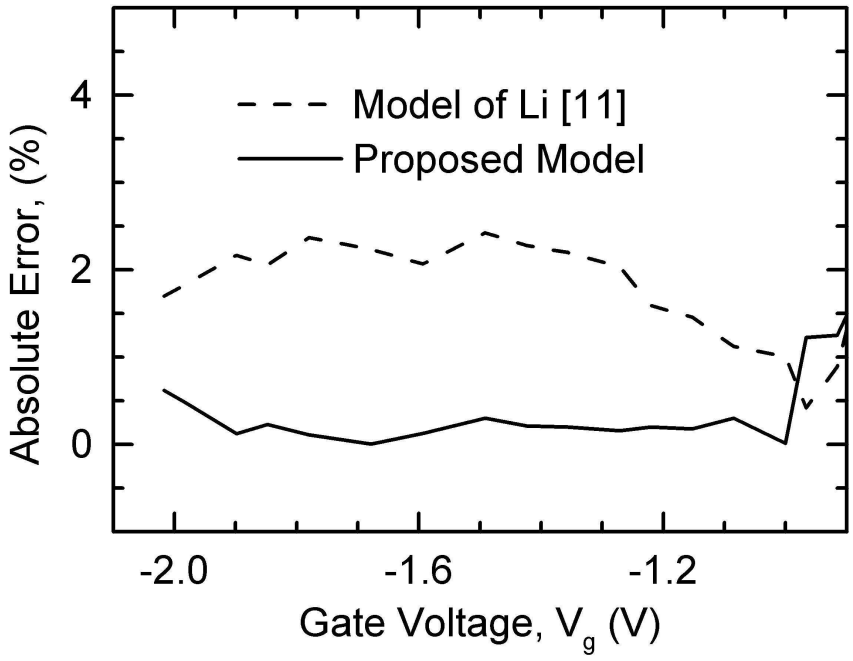

Figure 3.17: Error curve for Si_3N_4 as gate dielectric material.

3.4.2 Comparison of C-V Characteristics for Electrons

Four C-V curves are taken to evaluate the accuracy of our model and Li et al.'s model for electrons (n-MOS inversion and p-MOS accumulation). For each case two more C-V curves are developed. One from model of Ref. [11] taking λ=0.61 and another from our improved compact model determining λ from (3.7).

Fig. 3.18 shows experimental and simulated C-V for HfO_2 dielectric material [32]. We have used $N_d = 2 \times 10^{18}$ cm^{-3}, EOT = 1.87 nm and $\phi_b = 1.5$ eV. V_{FB} and N_d are calculated from the experimental C-V curve. We have V_{FB} = 0.35 V. λ from Eqn. 3.7 is 0.56. Here our model shows less error in strong accumulation region. Maximum error from model of Li et al. is 2.78% and from our model is 0.94% at V_g = 1.4 V. It is shown in Fig. 3.19. About 1.4% error is suppressed in our model.

Fig. 3.20 shows another C-V for HfO_2 dielectric material [33]. Here value of the parameters are $N_d = 5 \times 10^{17}$ cm^{-3}, EOT = 1.94 nm and $\phi_b = 1.5$ eV. V_{FB} and N_d are calculated from the experimental C-V curve. V_{FB} = 0.90 V is used. From Eqn. 3.7 λ is 0.57. Again our model has less error in strong accumulation region. Maximum error

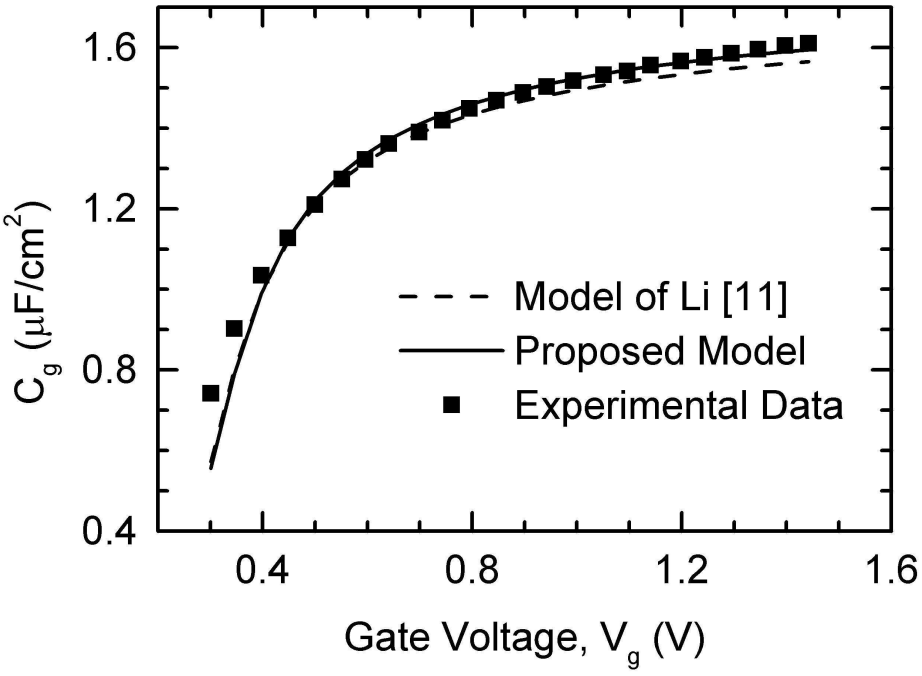

Figure 3.18: C-V curves for HfO_2 as gate dielectric material. Here doping density $N_d = 2 \times 10^{18}$ cm^{-3}, EOT = 1.87 nm.

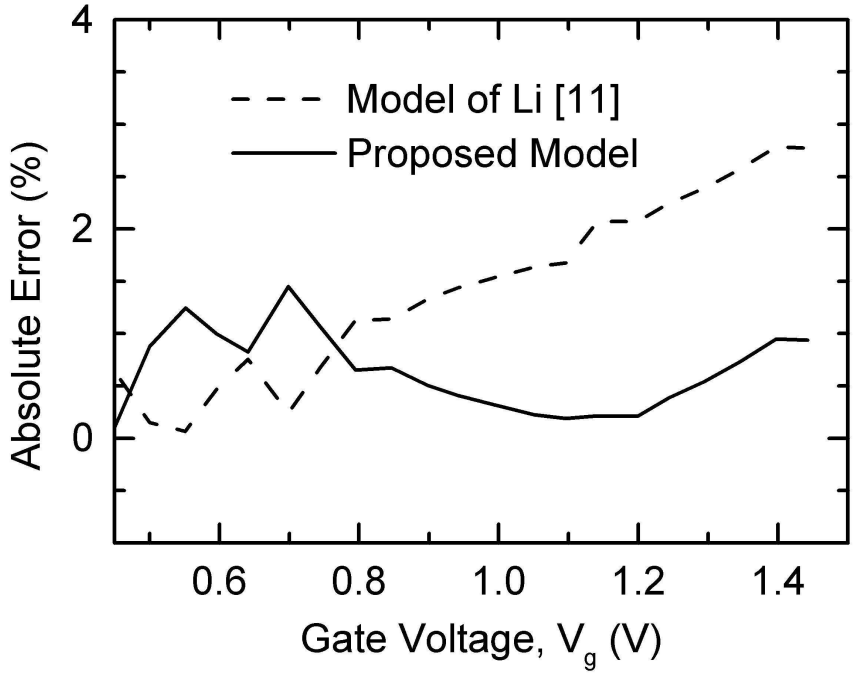

Figure 3.19: Error curve for HfO_2 as gate dielectric material.

from Li et al.'s model is 2.78% and from our model is 0.94% at V_g = 1.4 V. It is shown in 3.21.

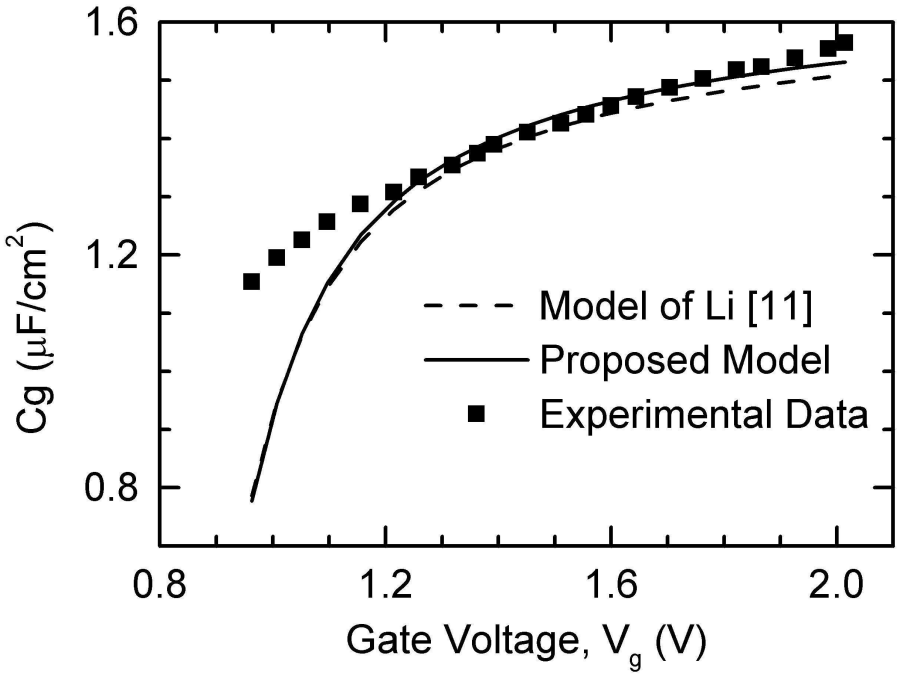

Figure 3.20: C-V curves for HfO_2 as gate dielectric material. Here doping density $N_d = 5 \times 10^{17}$ cm^{-3}, EOT = 1.94 nm.

Fig. 3.22 shows C-V for Y-O-Si dielectric material [29]. Parameter values are $N_d = 5 \times 10^{15}$ cm^{-3}, EOT = 1.17 nm and $\phi_b = 2.0$ eV. V_{FB} and N_d are calculated in the same way as above. V_{FB} = -1.63 V is used. From Eqn. 3.7 λ is 0.623. Our model has less error than the model of Li et al. Maximum error from Li et al.'s model is 2.78% and from our model is 0.94% at V_g = 1.4 V. Fig. 3.23 shows this result.

Fig. 3.24 shows C-V for Si_3N_4 dielectric material [31]. Parameter values are $N_d = 3.7 \times 10^{17}$ cm^{-3}, EOT = 1.56 nm and $\phi_b = 2.0$ eV. 3.7 gives λ to be 0.593. Once again our model has less error than model of Li et al. Maximum error from model of [11] is 2.78% and from our model is 0.94% at V_g = 1.4 V. Fig. 3.25 shows this result.

Explanation for C-V curves in positive gate voltage region is same as that of negative gate voltage region. Model of Li et al. underestimates the capacitance. It assumes that there is a small interfacial layer of SiO_2 between Si and gate oxide. But in case of pure high-k material this assumption is not valid. We should take real barrier height ϕ_b.

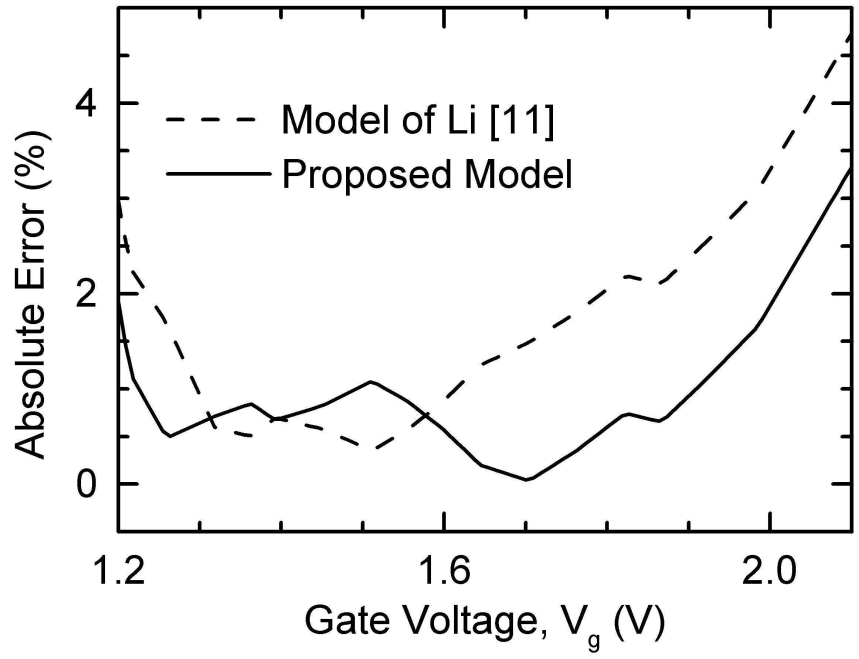

Figure 3.21: Error curve for HfO_2 as gate dielectric material.

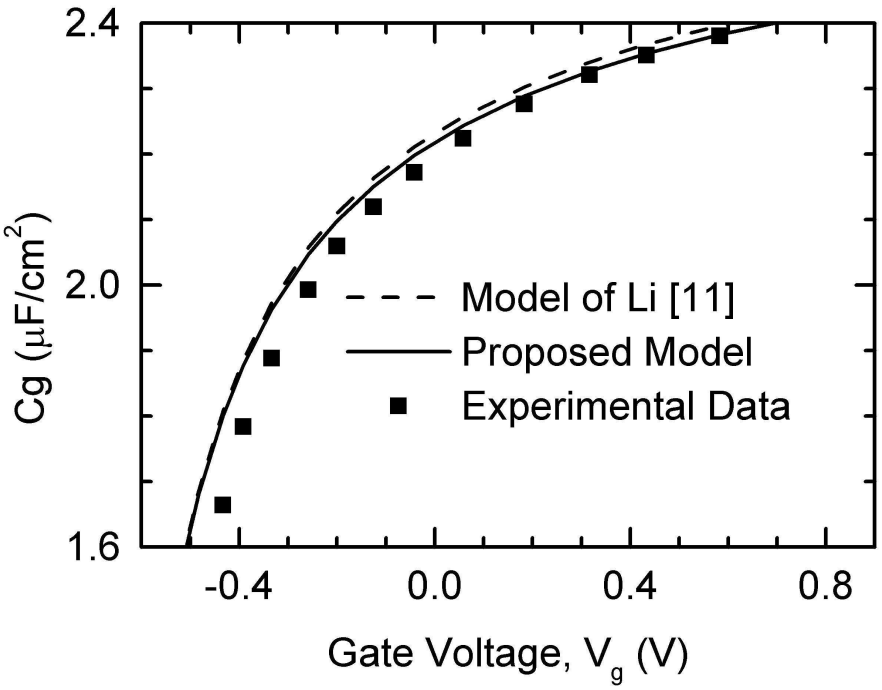

Figure 3.22: C-V curves for YOSi as gate dielectric material. Here doping density $N_d = 5 \times 10^{15}$ cm^{-3}, EOT = 1.17 nm.

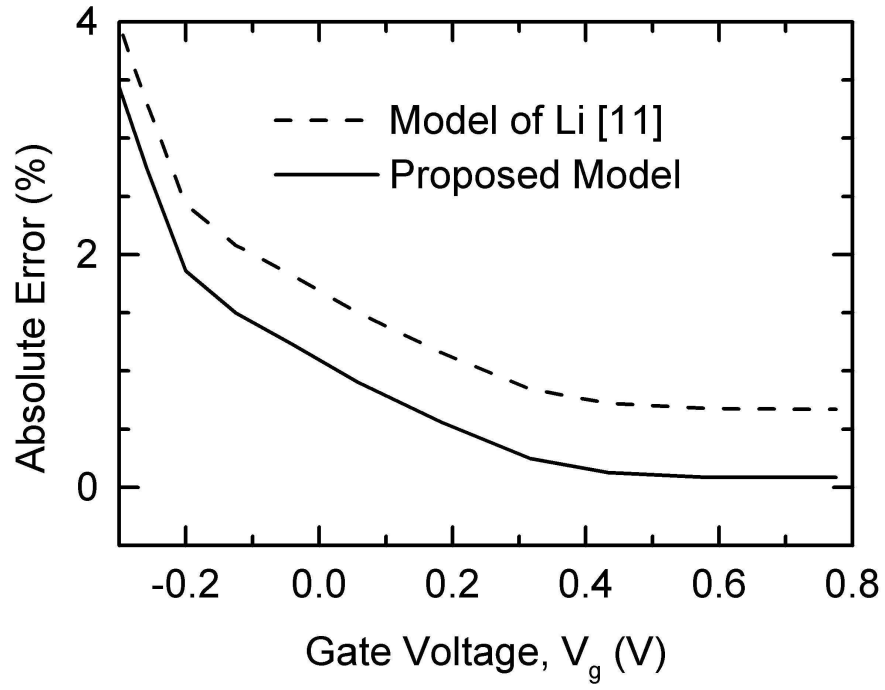

Figure 3.23: Error curve for YOSi as gate dielectric material.

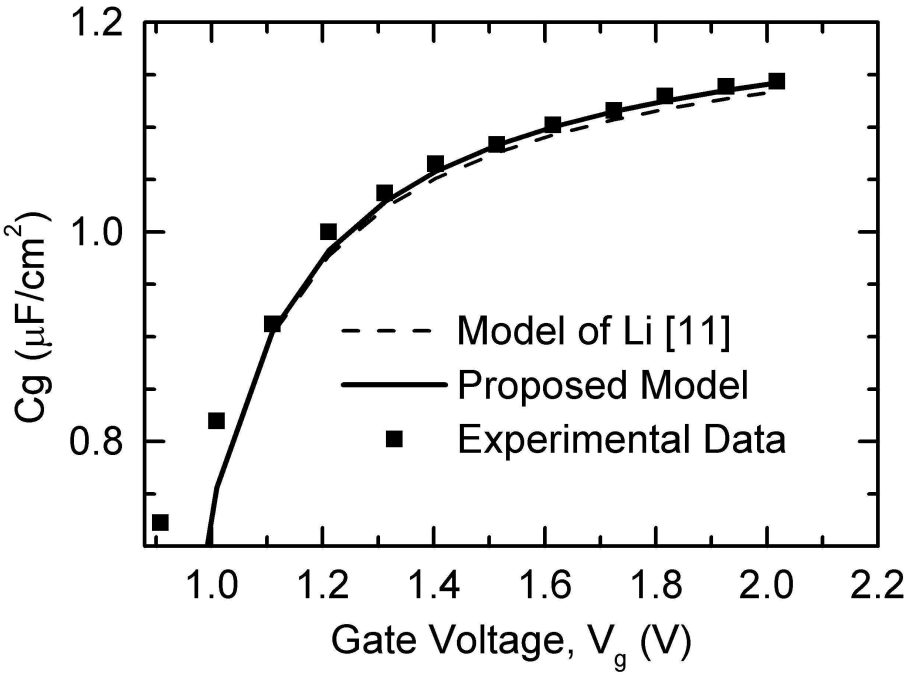

Figure 3.24: C-V curves for Si_3N_4 as gate dielectric material. Here doping density $N_d = 3.7 \times 10^{17}$ cm^{-3}, EOT = 1.56 nm.

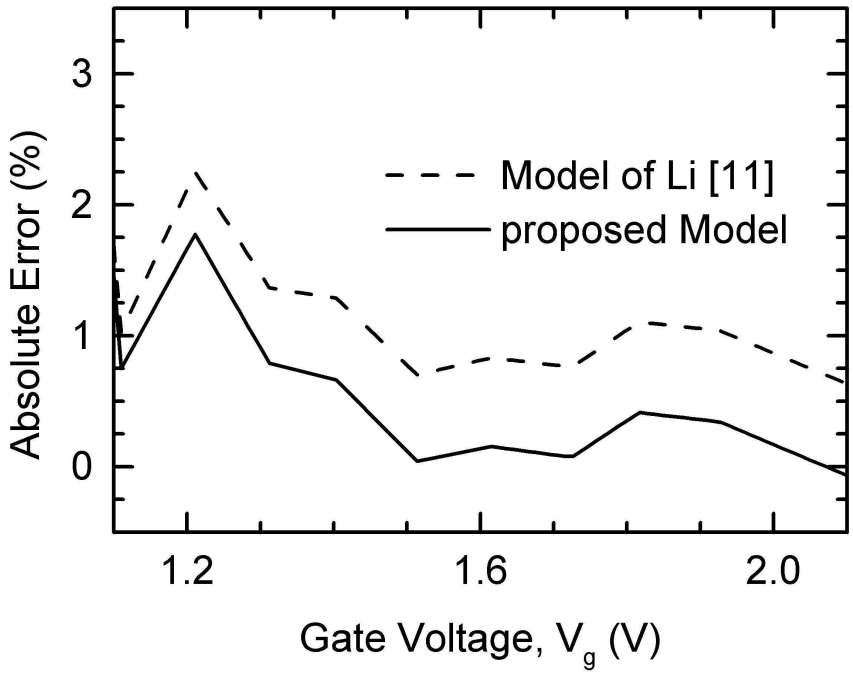

Figure 3.25: Error curve for Si_3N_4 as gate dielectric material.

Again doping concentration $N_{a,d}$ must also be considered for accurate modeling of C-V.

Chapter 4

Conclusion

An improved compact model is developed to simulate C-V curves with high-k gate dielectrics. It is based on previously published compact model. The exponent over oxide field of the 2/3 power law relationship ($E_1 \propto F_{ox}^{2/3}$) is supposed to vary with dielectric material properties and doping density of the bulk. Comparison of C-V curves obtained from both the models with experimental one shows validity of improved compact model.

4.1 Summary

Compact model is necessary in day to day life for accurately simulating C-V curves. MOSFETs are now most popular electronic device in silicon chip technologies. They are popular due to their low power consumption and less power-delay product than bipolar transistors. But capacitance play a vital role in determining performance of a MOSFET. For this reason many simulators are developed to obtain accurate C-V characteristics. Self-consistent simulators can simulate C-V curves with high accuracy but with the penalty of taking huge time. Compact models are developed to shrink this time. But compact models have their own limitations. Previously published compact model can simulate C-V curves only if there is SiO_2 in gate oxide or there is a small

interfacial layer of SiO_2 between gate dielectric and Si body.

Trend of modern MOSFET devices is to move from SiO_2 to high-k gate oxide. This improves leakage current and gate capacitance value in strong accumulation region. So we need a compact model that can simulate C-V MOS devices with high-k gate dielectrics correctly. The model presented in this thesis is capable of generating C-V curves with pure high-k dielectrics. One dielectric has different properties than the other. So it is necessary to consider different properties of these dielectric materials. One such property is barrier height. In previously published compact model high-k materials were simulated with barrier height value of SiO_2. This certainly does not give accurate result in all cases. On the other hand they negletted substrate doping densities. But C-V curves strongly depends on doping concentration in weak to moderate inversion and accumulation. So complete C-V curve needs this two effects to be taken into account. Our model incorporates both this effects and exponent over oxide field to calculate eigenenrgy is expressed as a function of these two. Two different equations are given to determine exponent for holes and electrons.

Finally eight C-V curves are taken to prove the validity of improved compact model. All the cases showed better result than general compact model. Error is suppressed in good amount for both holes and electrons. Error minimization is more for holes than electrons.

4.2 Probable Future Works

Our proposed improved compact model is valid for pure single layer high-k or multi-layered high-k dielectrics. If one or more layers are of low-k, then our model fails to simulate C-V curves accurately. Reason behind this is the limitation of our simulator used to calculate exponent value. This simulator can handle only one layer of dielectric. It is possible to have more simulation results with more than one layer of dielectric with other simulators. These results can easily combined with the present structure of

this model, and via the final model any number of layered dielectric C-V can be simulated.

Also our model fails to give accurate result in case of SiO_2 interfacial layer presence. If we can know the thickness of interfacial layer then special simulators can be used to find exponent value for total dielectric combination. With this interfacial layered MOSFET C-Vs can also be simulated.

Recently MOSFETs are entering in nanometer regime. So there are chances that oxide energy structure will not remain as smooth as in theory. These special conditions can also be incorporated in our compact model by evaluating exponent value. In all the cases only parameter that has to be changed is the exponent. Values of it can be determined and expressed as a function of certain parameters. With this function and existing compact model of ours, any type of gate dielectrics can be simulated.

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Appendix A

Flow chart for self-consistent model

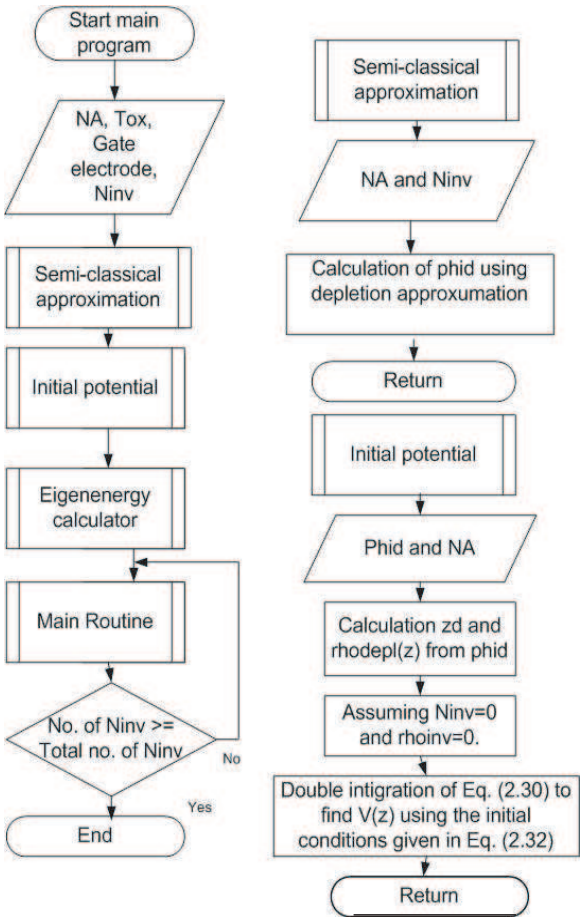

Figure A.1: Flow Chart for calculating self-consistent solution of eigenenergies.

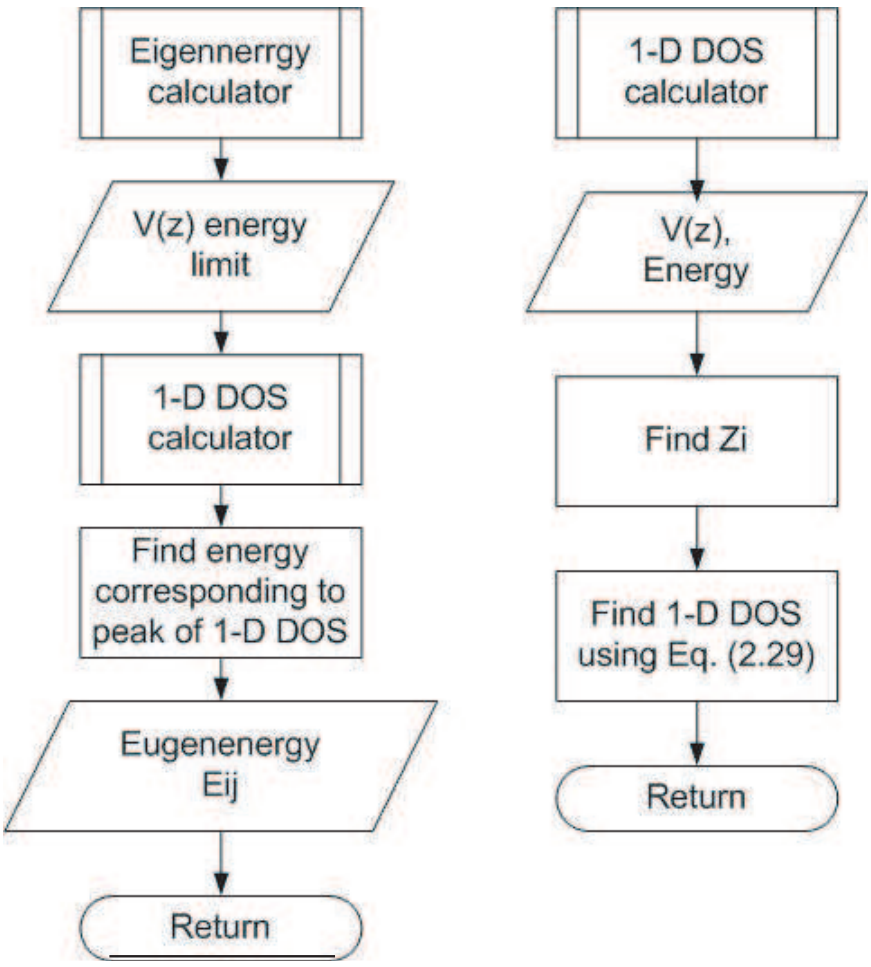

Figure A.2: Flow Chart for calculating self-consistent solution of eigenenergies (cintinued).

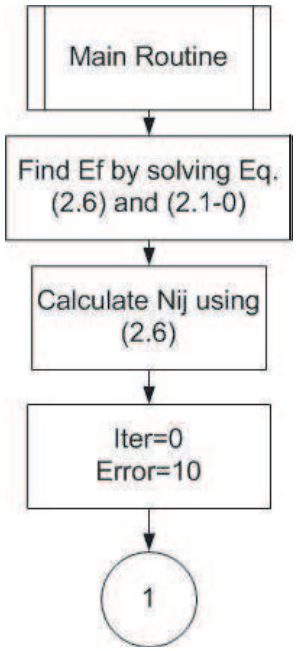

Figure A.3: Flow Chart for calculating self-consistent solution of eigenenergies (continued).

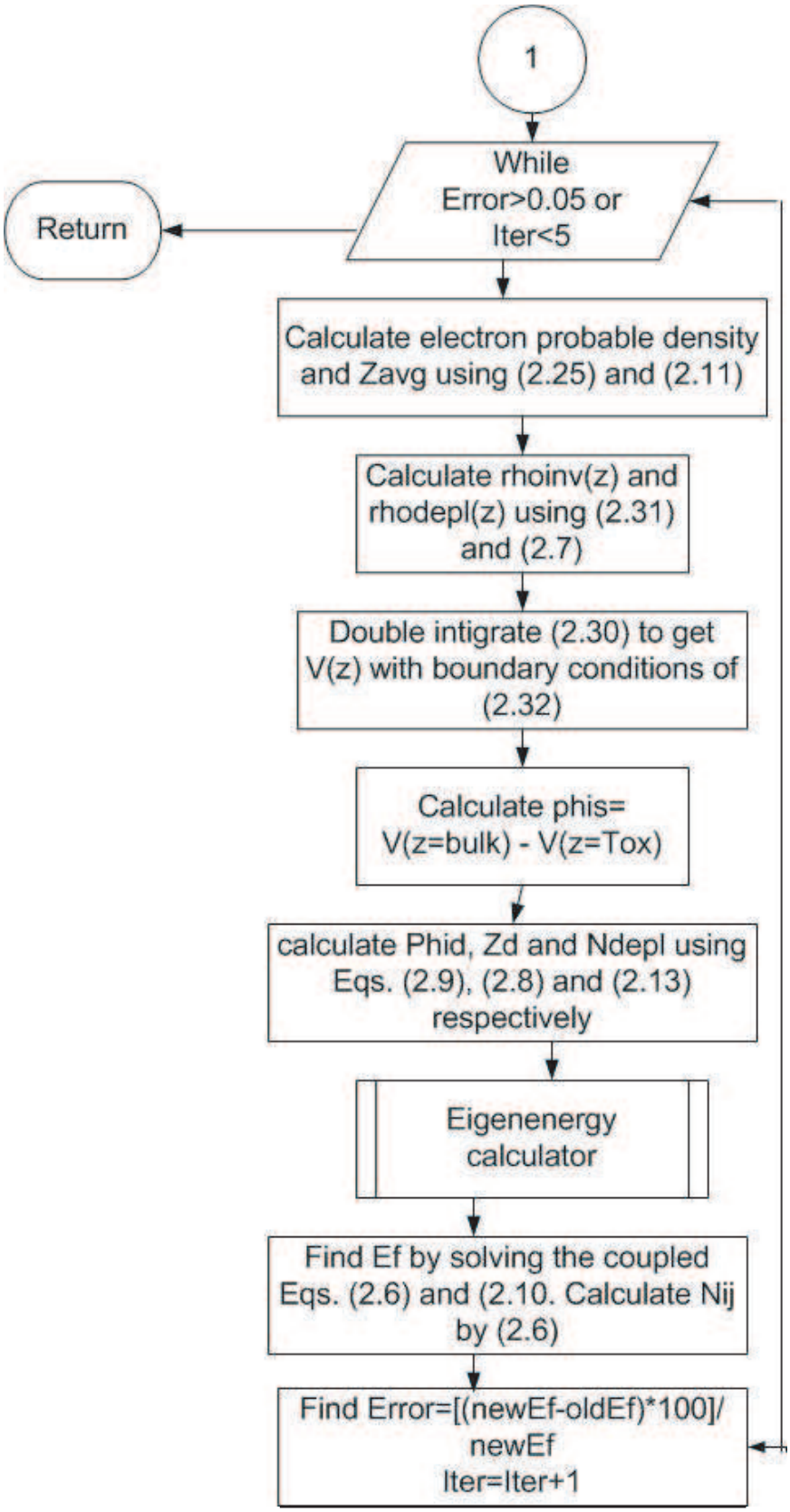

Figure A.4: Flow Chart for calculating self-consistent solution of eigenenergies (continued).

Appendix B

Flowchart for compact model

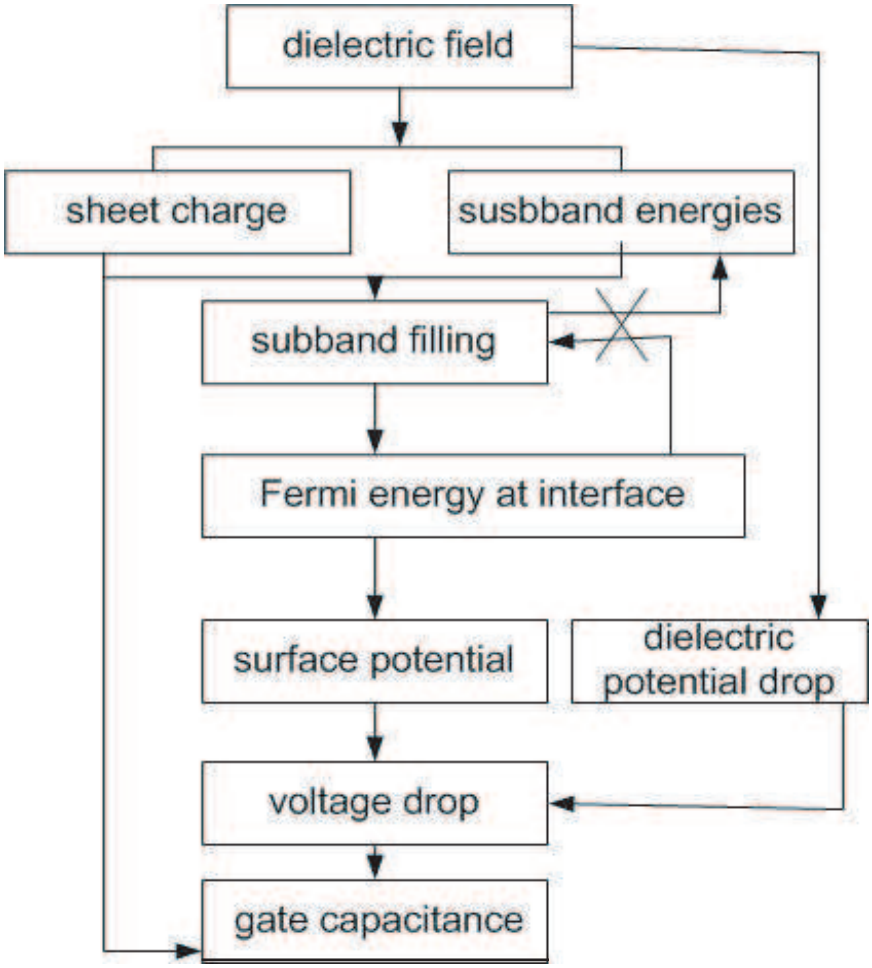

Figure B.1: Flow Chart for compact model.

Appendix C

Flowchart for improved compact model

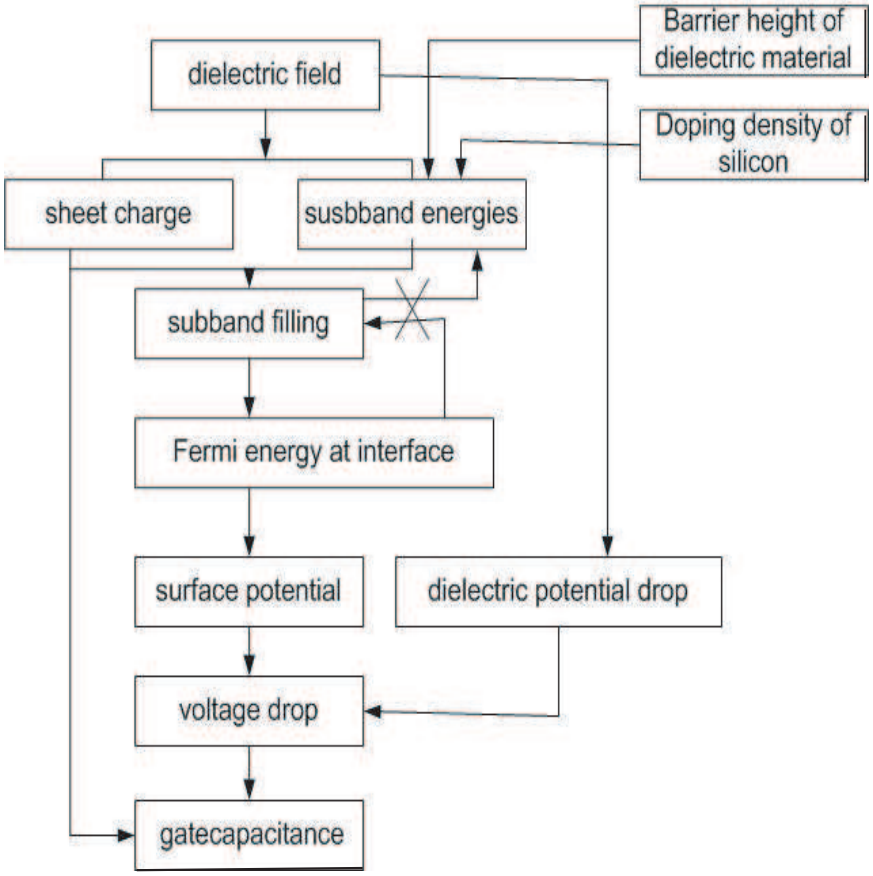

Figure C.1: Flow Chart for improved compact model.